A LOW-RIPELLE CHARGEPUMP CIRCUIT FOR HIGH VOLTAGE APPLICATIONS

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Abstract
The subject of this paper is a fully integrated chargepump circuit with a very low output voltage ripple. At a supply voltage of 30V the chargepump can source 1mA at an output voltage of 40V. Two simple modifications to the classical chargepump circuit give a substantial reduction of the output voltage ripple.

1. Introduction

DMOS devices are very attractive for the use in power stages because, unlike bipolar transistors, they do not suffer from secondary breakdown. In BCD technologies, usually only n-type DMOS devices are available for both the upper and lower power transistors in an output stage. Two examples of power stages are shown in figure 1.1. In order to achieve a low "on"-resistance the gate of the high-side DMOS transistor must be about 10V higher than the supply voltage V_p. This voltage can be generated on-chip by a so-called chargepump [1-3]. In the voltage-follower output shown in figure 1.1(a), the gate of the DMOS transistor forms a capacitive load.

Sometimes it can be advantageous to use a current-mode output [4]. A current-mode power stage is shown in figure 1.1(b). The output transistors are part of a current mirror with very large mirror-ratio, for example 1:1000. In this case, a chargepump is needed that can provide the required gate voltage while loaded with a current up to a few milliampères.

2. Principle of Operation

Most integrated chargepump circuits are based on the chargepump circuit proposed by Dickson [5]. A voltage doubler based on this circuit is shown in fig 2.1. The pump capacitor C_pump is driven with a square wave voltage V_o. When the clock is low (V_o=0), the pump capacitor C_pump is charged through diode D_1 while diode D_2 is reverse biased. When the clock
is high \((V_\Phi = V_p)\), diode \(D_1\) is reverse biased and a part of the charge on \(C_{\text{pump}}\) will be transferred through diode \(D_2\) to the storage capacitor \(C_{\text{store}}\).

In steady state the peak output voltage \(V_o\) of the chargepump can be approximated by:

\[
V_{o,\text{peak}} = V_p + V_\Phi - 2 \cdot V_d - \frac{I_o}{f \cdot C_{\text{pump}}}
\]

where \(V_p\) is the supply voltage, \(V_\Phi\) is the clock amplitude, \(V_d\) is the forward bias voltage of the diodes, \(I_o\) is the load current and \(f\) is the clock frequency. Due to the discharge of the storage capacitor \(C_{\text{store}}\) there will also be a voltage ripple at the output which can be approximated by:

\[
V_{o,\text{ripple}} = \frac{I_o}{f \cdot C_{\text{store}}}
\]

If the load current \(I_o\) is constant, the output voltage will ideally have a sawtooth shape as is indicated in figure 2.1.

The voltage ripple can become quite high when the output current is high. A simple solution to reduce the voltage ripple is to use a larger storage capacitor. However, this will require more chip area and it will make the startup behavior of the chargepump slower [6].

### 3. Improved Chargepump Operation

After analyzing the cause of the output voltage ripple, a more elegant solution was found. The steep rising edge is caused by the almost instantaneous charge transfer between the pump capacitor \(C_{\text{pump}}\) and storage capacitor \(C_{\text{store}}\) is. The almost linear voltage droop is caused by the load current \(I_o\) discharging the storage capacitor \(C_{\text{store}}\).

A simple reduction of the voltage ripple can be obtained by using a double phase chargepump shown in figure 3.1(a). This chargepump has two pump capacitors, driven in antiphase. The two pump capacitors are half the size of the single pump capacitor in the original chargepump. Therefore the area of the circuit hardly increases.

The increase in performance however is significant. The resulting output voltage is a sawtooth with half the amplitude and twice the frequency of the original output voltage as illustrated schematically in figure 3.1(a).

Another simple reduction of the voltage ripple can be obtained by driving the chargepump with a current source instead of a squarewave voltage as shown in figure 3.1(b). If the driving current is twice the load current, the output voltage waveform will change to a triangular wave with half the amplitude of the original sawtooth output voltage as illustrated schematically in figure 3.1(b). A further advantage of this method
is that the peak currents through the diodes will be much smaller resulting in more relaxed design criteria.

A combination of both modifications will result in an even better chargepump which, in theory has no voltage ripple at all. This can be seen as follows, in the first half clock period, one side of the pump delivers a constant current to the storage capacitor $C_{\text{store}}$, while the other side is recharging. In the second half the situation is reversed. Consequently, a constant current is delivered to the storage capacitor $C_{\text{store}}$. If this current is made equal to the load current $I_o$, the charge on the storage capacitor is kept constant and therefore the output voltage will not be change.

The basic idea for reducing the ripple voltage is to make the charge transfer towards the storage capacitor more gradual. In practice an ideal ripple-free output voltage can, of course, not be achieved due to all kinds of parasitic effects. However, a significant reduction in voltage ripple can easily be achieved with only a small increase in circuit complexity. Moreover, current drivers can be realized with smaller transistors than voltage drivers since they do not have to be able to provide the large peak currents that result from steep voltage edges. Therefore, even a reduction in area can be achieved. Clearly, these voltage reduction methods are also applicable to multiple stage chargepumps.

4. Implementation

A chargepump prototype has been realized in a DMOS process. The pump has a double phase structure as shown in figure 3.1(a). The schematic of one of the driver circuits is shown in figure 4.1. It consists of two current mirrors $M_{7,8}$ and $M_{9,10}$ working at a supply voltage of 30V. The current mirror $M_{9,10}$ is constructed with so-called extended-drain PMOS (EPMOS) transistors.

When the clock $V_\phi$ is high, DMOS transistor $M_3$ is conducting and current mirror $M_{9,10}$ is driven, so a current $I_{\text{out}}$ is sourced at the output. When the clock $V_\phi$ is low, transistor $M_4$ is conducting and current mirrors $M_{5,6}$ and $M_{7,8}$ are driven, so a current $I_{\text{out}}$ is sunk at the output. The magnitude of the output current $I_{\text{out}}$ is controlled by an external source $I_{\text{external}}$. The chargepump can operate in both single-phase and double-phase mode by driving the two sides in phase or in anti-phase respectively. Further, both voltage-driven and current-driven operation can be chosen by changing the control current $I_{\text{external}}$. The driver has been designed in such a way that it can deliver a current much larger than the load current in order to approach voltage-driven operation. If only current-driven operation is required the driver circuit can be made much smaller. Consequently, all four operation modes described earlier can be used.

The complete chargepump circuit consists of a relaxation oscillator running at $1.67\text{MHz}$, some control logic, two driver circuits, two pump capacitors of $16.7pF$ one storage capacitor of $300pF$, and four low-substrate-current diodes. The circuit requires two supply voltages of
The bottom plate of the storage capacitor is connected to the power supply, so the voltage across this capacitor will be in the range of 10V. Therefore the storage capacitor can be made with thin gate-oxide. The pump capacitors are charged with the full supply voltage and are therefore realized with a thick oxide.

5. Measurement Results

The measured output voltage waveforms in the four operation modes are shown in figure 5.1. The load current $I_{load}$ was 1.0mA in all cases. As can be seen, the reduction in voltage ripple between the (original) voltage-driven, single-phase mode and the current-driven, double-phase-mode is considerable. It is expected that a further reduction in voltage ripple is possible when an improved driver design is used. The total area of the chargepump is about 1.2mm$^2$. A microphotograph of the prototype chip is shown in figure 5.2.

6. Conclusion

A fully integrated chargepump has been designed for a high output current with a low voltage ripple. This low voltage ripple can be obtained with only a small increase in complexity of this circuit compared to the conventional solution. The effectiveness of the ripple reduction has been demonstrated with measurements.

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8. References