A High-Voltage Class-D Power Amplifier with Switching Frequency Regulation for Improved High-Efficiency Output Power Range

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Abstract — This paper describes the power dissipation analysis and the design of an efficiency-improved high-voltage class-D power amplifier. The amplifier adaptively regulates its switching frequency for optimal power efficiency across the full output power range. This is based on detecting the switching output node voltage level at the turn-on transition of the power switches. Implemented in a 0.14µm SOI BCD process, the amplifier achieves 93% efficiency at 45W output power, >80% power efficiency down to 4.5W output power and >49% efficiency down to 0.45W output power.

Keywords — Class-D amplifier, Switching frequency, Power efficiency, Switching loss, Hard switching, Soft switching, Efficiency optimization, Piezo driver, High voltage

I. INTRODUCTION

High-voltage, high-power class-D amplifiers have gained popularity for audio amplification [1-6]. Their higher power efficiency compared to linear amplifiers enables the use of small or even no heat sinks when delivering full power. For the application area of piezoelectric-actuator drivers [7], where the actuator loads are largely capacitive and the reactive power can go to several tens of Watts, class-D designs have also demonstrated very high peak efficiency [8].

However, high power efficiency should be achieved at both maximum power and at average power. This is necessitated by the relatively high peak-to-average ratio of
audio signals [9]. Consequently the average power level that the amplifier is typically operating at can be orders of magnitude lower than the maximum output power.

Aiming for optimized power efficiency across a certain output power range, the output transistor size [10] or the switching frequency, $f_{sw}$ [2] can be chosen for a tradeoff between low- and high-power efficiency. Fixing the transistor size and $f_{sw}$ results in either the low- or high-power efficiency being suboptimal. Adaptive techniques for changing the power transistor size [11] or $f_{sw}$ [12], [13] have been proposed for further efficiency enhancement. However, the dynamic power stage activation in [11] is not suitable for high-voltage applications because the parasitic capacitance at the output node of the power stage is still present for the inactive part of the power stage, resulting in the same high switching loss. Varying $f_{sw}$ according to the output current only [12], [13] is also suboptimal since the actual power dissipation mechanisms are highly dependent on other circuit operating conditions such as the output inductor ripple current, as will be explained in the following section.

In this paper we propose a switching frequency regulation technique that minimizes power dissipation from idle to maximum output power [14]. This is achieved by detecting the output switching node voltage level at the turn-on transition of the power switches. This information is directly related to the dissipation sources and is inherent for getting to the optimal $f_{sw}$ and in turn minimal dissipation, independent of circuit operating conditions affecting the output inductor ripple current. Adding to [14], the class-D power stage dissipation sources are analyzed and modeled in detail. Also, more detailed circuit implementations are discussed. In section II we show a detailed modeling of the dissipation sources in a high-voltage class-D power stage. The proposed $f_{sw}$ regulation for efficiency improvement is described in section III. In section IV, the topology and circuit realization is described.
Section V discusses the measurement results and in section VI the conclusions are drawn.

II. CLASS-D POWER STAGE DISSIPATION MODELLING

A basic class-D power stage topology is shown in Fig. 1. Two N-type DMOSFETs are used as power switches and their on/off state is controlled by two gate driver circuits. Typically the maximum $V_{ds}$ of the DMOSFETs is much higher than their $V_{gs}$, therefore the gate driver supply $V_{DD}$ is much lower than the output stage supply $V_{DDP}$. Here we use the three-line ground symbol to represent the off-chip ground, as to distinguish it from the on-chip power ground PGND. This is because parasitic inductances exist between the on-chip and off-chip power supplies and they also poses significant design challenges related to on-chip power supply bounce [1], [6], [8]. We choose a single-ended power stage here because a DC bias voltage is required for the piezo-actuator load to deform bi-directionally [7]. The following dissipation analysis is also directed to this single-ended topology. Bridge-tied-load topologies can give different results, yet all the dissipation sources listed here still apply.

The current $I_L$ flowing through the power inductor $L_{out}$ can be divided into two parts: the average load current within one switching cycle with value $I_{out}$ and the inductor ripple current with amplitude $I_{rip}$ expressed as [15]:

$$I_{rip} = \frac{V_{DDP} D (1-D)}{2 f_{sw} L_{out}}$$

(1)

where $f_{sw}$ is the class-D switching frequency and $D$ is the $V_{pwm}$ duty cycle. As we can see from (1), $I_{rip}$ is influenced by numerous circuit operating parameters. This makes the ratio between $I_{out}$ and $I_{rip}$ also dependent on these parameters. Yet the $I_{out}$-
Irip ratio is important for identifying the different dissipation contributions at changing output power levels, as will be discussed in the following subsections.

A. Class-D Power Stage Dissipation Sources

The main dissipation sources in a class-D power stage are listed in TABLE I. Among them, conduction loss $P_{\text{con}}$ is due to $I_{\text{out}}$ (assumed to be constant in this analysis) flowing through the on resistance of the power transistors ($r_{\text{on}}$) and the equivalent series resistance of $L_{\text{out}}$ ($r_{\text{esr}}$),

$$P_{\text{con}} = I_{\text{out}}^2 (r_{\text{on}} + r_{\text{esr}})$$  \hspace{1cm} (2)

Ripple loss $P_{\text{rip}}$ is caused by the $I_{\text{rip}}$ conduction in $r_{\text{on}}$ and $r_{\text{esr}}$, as well as the magnetic core loss in $L_{\text{out}}$. Assuming $I_{\text{out}}$ is constant during one switching cycle with the triangle $I_{\text{rip}}$ superimposed on it, the conduction loss contribution of $I_{\text{rip}}$ can be expressed as,

$$P_{\text{rip,cond}} = \frac{1}{3} I_{\text{rip}}^2 (r_{\text{on}} + r_{\text{esr}})$$  \hspace{1cm} (3)

Here the $1/3$ coefficient for $P_{\text{rip,cond}}$ comes from the triangle wave nature of $I_{\text{rip}}$, compared to the constant $I_{\text{out}}$ used in $P_{\text{con}}$ in (2).

There is also magnetic core loss, related to the hysteresis of the B-H loop of the inductor core material. This loss is the unrecoverable part of the energy required for the changing magnetization of the core material and is expressed as [16],

$$P_{\text{rip,core}} = K(V_{\text{ol}})(f_{\text{sw}})^x(\Delta B)^y$$  \hspace{1cm} (4)

where $K$ is a constant for core material, $V_{\text{ol}}$ is the core volume, $x$ is the power factor for $f_{\text{sw}}$ and $y$ is a power factor for the changing magnetic flux density with amplitude $\Delta B$. The changing magnetic field $\Delta H$, which varies together with $\Delta B$ following the B-H curve, is directly proportional to $I_{\text{rip}}$. Thus by adopting $x=1$ and $y=2$ as a simplified power factor [18], (4) can be rewritten using $I_{\text{rip}}$ as.
with $r_{eq} = 3K(VoI)f_{sw}$ being the equivalent resistance for the core loss contribution. It is worth noting that even though $r_{eq}$ is proportional to $f_{sw}$, $P_{\text{trip,core}}$ is still inversely proportional to $f_{sw}$, because $I_{\text{rip}}$ is inversely proportional to $f_{sw}$ according to (1).

Further combining the $I_{\text{rip}}$-induced conduction loss (3) and magnetic core loss (5),

$$P_{\text{trip}} = \frac{1}{3} I_{\text{rip}}^2 (r_{on} + r_{esr} + r_{eq})$$  \hspace{1cm} (6)$$

Gate driver loss $P_g$ results from charging/discharging the gate capacitance of $M_{HS}/M_{LS}$ when turning $M_{HS}/M_{LS}$ on/off. $P_g$ for $M_{HS}$ and $M_{LS}$ combined can be expressed as:

$$P_g = Q_g V_{DD} f_{sw}$$  \hspace{1cm} (7)$$

where $Q_g = \int_{V_{GND}}^{V_{DD}} C_g(V) dV$ with $C_g$ the total gate capacitance of $M_{HS}$ and $M_{LS}$. Total gate charge instead of the gate capacitance is adopted here for easier and more precise power loss calculation because the parasitic capacitances of a power MOSFET show large variations over changing bias conditions [19].

Both the capacitive loss $P_{\text{cap}}$ and the switching loss $P_{\text{sw}}$ are induced by the switching at the pulse-width-modulated (PWM) output node $V_{pwm}$. With a high-voltage $V_{DDP}$, $P_{\text{cap}} + P_{\text{sw}}$ can be significant. Yet whether these two dissipation sources exist, depends on the $V_{pwm}$ switching waveforms and consequently on the $I_{\text{out}} - I_{\text{rip}}$ amplitude, as will be discussed in detail in the following.

**B. $V_{pwm}$-Switching-Induced Power Loss Analysis**

Depending on the inductor current direction and amplitude at the moment of switching, three $V_{pwm}$ switching types can be identified as follows (using $V_{pwm}$ low-to-high transitions for illustration):
1) Hard switching (HSw). As shown in Fig. 2, the inductor current $I_L$ is flowing out of the power stage as $M_{LS}$ is turned off at $t_0$. During the dead time $t_d$, when both $M_{HS}$ and $M_{LS}$ are kept off, $I_L$ has nowhere to go but through the body diode of $M_{LS}$. As a result $V_{pwm}$ will stay near $PGND$. This remains until $M_{HS}$ is turned on at $t_1$ when $t_d$ is finished. The switching transition only begins when the current $I_{HS}$ in $M_{HS}$ is large enough to provide the sum of three currents: 1. $I_{cap}$ for charging $C_{par}$. 2. the reverse-recovery current $I_{rr}$ [4] of the body-diode of $M_{LS}$, and 3. the inductor current $I_L$. Of these currents that contribute to $M_{HS}$ dissipation, the $I_{cap}$ contribution can be expressed as:

$$P_{cap, HSw} = \frac{1}{2} Q_o V_{DDP} f_{sw}$$

(8)

where $Q_o = \int_{PGND}^{V_{DDP}} C_{par}(V) dV$ when $M_{HS}$ is on while $M_{LS}$ is off.

As for the contribution of $I_{rr}$ and $I_L$, the transition time from $t_1$ to $t_2$ is determined by the gate driver pull-up strength [8] and thus the V-I overlap part contributed by $I_L$ will be dependent on the gate driver design. To simplify the modeling of $P_{sw}$, we assume that the gate driver pull-up strength is large enough to make the transition very fast and to satisfy $I_L(t_2-t_1) << Q_{rr}$ (the reverse recovery charge). Then we get

$$P_{sw, HSw} = \frac{1}{2} Q_{rr} V_{DDP} f_{sw}$$

(9)

$P_{cap, HSw} + P_{sw, HSw}$ then will be the total $M_{HS}$ dissipation during the hard switching transition. The reverse recovery charge $Q_{rr}$ is the minority charge stored in the body diode of $M_{HS}/M_{LS}$ that needs to be flushed out [4], when the forward conducting current flowing through the diode stops. The value of $Q_{rr}$ is related to the amplitude of the initial conducting current, the speed at which this current decreases as well as the technology in which the DMOS transistor is implemented.

2) Soft switching (SSw). The switching dynamic changes when $I_L$ is flowing into the power stage at the transition time, as shown in Fig. 3. In this case when $M_{LS}$ is turned
off at $t_o$, $I_L$ immediately begins to charge $C_{par}$ and $V_{pwm}$ begins to rise. If $I_L$ is large enough to satisfy

$$I_L * t_d \geq Q_o \quad (10)$$

where $Q_o = \int_{PGND}^{V_{DDP}} C_{par}(V) dV$ when both $M_{HS}$ and $M_{LS}$ are off, the switching transition will finish within the dead time at $t_1$ before $M_{HS}$ is turned on at $t_2$. No V-I overlap in the active devices exists and thus $P_{cap,SSW} + P_{sw,SSW} = 0$.

3) Partial soft switching (PSSW). Same as in the case of lossless soft switching, $I_L$ is flowing into the power stage at the transition time, as shown in Fig. 4. When $M_{LS}$ turns off, $I_L$ also immediately begins to charge $C_{par}$, thus $P_{sw,PSSW} = 0$. However, if the value of $I_L$ is too low to satisfy (10), $C_{par}$ cannot be charged to $V_{DDP}$ within $t_d$. $M_{HS}$ is turned on to finish the rest of the transition with $P_{cap,PSSW}$ loss expressed as:

$$P_{cap,PSSW} = \frac{1}{2} F^2 Q_o V_{DDP} f_{sw} \quad (11)$$

where $F$ represents the ratio of the remaining $V_{pwm}$ transition that has to be finished by the active power switches and is approximated here as:

$$F = (Q_o - I_L t_d) / Q_o \quad (12)$$

To summarize the combined $P_{cap} + P_{sw}$ for the above three switching transition scenarios, we define the inductor current in the direction of flowing out of the power stage to be positive, then

$$P_{cap} + P_{sw} = \begin{cases} 
\frac{1}{2} (Q_{rr} + Q_o) V_{DDP} f_{sw} & \text{if } I_{out} - I_{rip} > 0 \\
0 & \text{if } I_{out} - I_{rip} \leq 0 \text{ and } |I_{out} - I_{rip}| t_d \geq Q_o \\
\frac{1}{2} F^2 Q_o V_{DDP} f_{sw} & \text{if } I_{out} - I_{rip} \leq 0 \text{ and } |I_{out} - I_{rip}| t_d < Q_o 
\end{cases} \quad (13)$$

As for the $V_{pwm}$ high-to-low transition, $I_L$ now equals $I_{out} + I_{rip}$, which will be always flowing out of the power stage for positive $I_{out}$. This is a lossless soft switching transition when $(I_{out} + I_{rip}) t_d \geq Q_o$ is satisfied, which is typically the case.
Considering the complete switching cycle with a positive \( I_{\text{out}} \) as shown in Fig. 5, a higher \( I_{\text{rip}} \) amplitude than \( I_{\text{out}} \) results in bidirectional \( I_L \) and consequently both switching transitions are soft switching (Fig. 5(a)), with partial soft switching for the low-to-high transition still possible. On the other hand, a lower \( I_{\text{rip}} \) amplitude than \( I_{\text{out}} \) results in unidirectional \( I_L \), which means the low-to-high transition is hard switching (Fig. 5(b)).

### C. Verification of Loss Analysis

With analytical expressions for each of the dissipation sources listed in TABLE I as in (2), (6), (7) and (13), a comparison can be made between transistor-level power dissipation simulation and the analytical model. For the verification, we only consider the power loss of the transistors, i.e. \( r_{\text{esr}} \) and \( r_{\text{eq}} \) of the power inductor will not be considered yet. TABLE II shows a summary of the power stage design parameters [8] which have been used in both simulation and analytical models, while TABLE III lists the main parameters associated with the power DMOSFETs used in the analytical model.

Fig. 6 shows the comparison between the transistor-level simulation results and the analytical model, with two different \( I_{\text{out}} \) settings. For the simulations each \( I_{\text{out}} \) is set at a constant DC output current. The analytical model predicts the dissipation of the power switches well across the three different switching scenarios, with \( f_{\text{sw}} \) varied for getting to different \( I_{\text{rip}} \) such that all three scenarios are covered. The main discrepancy between the analytical model and the simulation lies in the PSSw region. This is due to the nonlinear \( C_{\text{par}} \), which makes the remaining voltage and charge ratio \( F \) in (12) not precise.

When comparing Fig. 6(a) and Fig. 6(b), we can observe that there exists a minimum power dissipation for each \( I_{\text{out}} \) case, with different optimal \( f_{\text{sw}} \) corresponding
to them. This further motivates us to investigate when $f_{sw}$ is optimal and how to get to it, as will be discussed in the next section.

III. EFFICIENCY IMPROVEMENT WITH SWITCHING FREQUENCY REGULATION

A. Dissipation Sources versus Switching Frequency

Using the analytical loss model developed in section II, the total dissipation $P_{total}$ and each of its contributing sources can be analyzed under different load conditions with varying $f_{sw}$. To identify the contributions, we first exclude the magnetic core loss of the output inductor, setting $P_{trip, core}=0$. The core loss is highly dependent on the type and size of the chosen inductor, and its effect will be added separately in the next section.

Fig. 7 shows the contributing dissipation sources for a low output power ($I_{out}=100mA$, $D=0.5$). As we can see from Fig. 7, because $P_{trip}$ is the dominating loss at low $f_{sw}$, $P_{total}$ can be significantly decreased with increasing $f_{sw}$. This trend continues until the gate driver loss $P_g$ becomes comparable with that of $P_{trip}$ and counteracts the decreasing $P_{trip}$. Consequently $P_{total}$ flattens out for higher $f_{sw}$. Further increasing $f_{sw}$ across the SSw boundary causes $P_{sw}+P_{cap}$ to rise significantly due to the high $V_{DDP}$.

With the output power increased to a medium level as shown in Fig. 8 ($I_{out}=400mA$, $D=0.5$), the same trend can be seen with $P_{total}$ decreasing together with $P_{trip}$ for increased $f_{sw}$. The SSw boundary is shifted to a lower $f_{sw}$ here because the necessary $I_{trip}$ to achieve SSw has increased due to the higher $I_{out}$. Also because of this lower $f_{sw}$ for achieving SSw, $P_g$ is insignificant compared to the other losses and the immediate increase in $P_{sw}+P_{cap}$ becomes the main dissipation source at higher $f_{sw}$. As can also be seen in Fig. 8, minimum $P_{total}$ is at a frequency slightly higher than the SSw boundary. This is because the decrease in $P_{trip}$ has a stronger effect than the
increase in $P_{sw} + P_{cap}$ in the PSSw region. Yet the decrease is insignificant, considering the constant $P_{con}$ that constitutes the larger part of $P_{total}$. In general, the minimum in the dissipation curve (assuming negligible $P_{g}$) is reached for $d(P_{trip})/d(f_{sw}) = - d(P_{sw} + P_{cap})/d(f_{sw})$. Since this latter term is very sensitive to $f_{sw}$ in the PSSw region, this explains why the minimum dissipation is very close to the soft switching boundary, which was already observed in Fig. 6.

When the output power further increases as shown in Fig. 9 ($I_{out}=800mA$, $D=0.5$), SSw cannot be achieved within the $f_{sw}$ range. Also, due to the high $V_{DDP}$, $P_{sw} + P_{cap}$ increase significantly with increasing $f_{sw}$. This makes the $P_{trip}$ contribution not important and thus increasing $f_{sw}$ is not beneficial. In this case the class-D amplifier should operate with the lowest possible $f_{sw}$.

The analysis made above can be summarized into two points, 1) When soft switching is possible, increasing $f_{sw}$ till the SSw boundary is beneficial to lower $P_{trip}$ and in turn $P_{total}$. Dissipation at that frequency is close to minimal. 2) When SSw cannot be realized, minimum $P_{total}$ is achieved at the lowest $f_{sw}$, where $P_{sw} + P_{cap}$ is the lowest. Based on these two points, achieving minimum dissipation across the full output power range means the class-D switching transitions should be at the SSw boundary whenever possible. With SSw conditions highly dependent on both $I_{out}$ and $I_{rip}$, and $I_{rip}$ influenced by numerous factors (e.g. $> 5\times$ variation in the 0.05-0.95 duty cycle range), an intelligent way to regulate $f_{sw}$ to the SSw boundary is required.

B. Output Inductor Loss Considerations

In the analysis made above, only the power loss from the output power transistors was considered. Yet the magnetic core loss of the output inductor can also be significant, especially when the inductor has to be compact. We take a Coilcraft MSS1278T 100µH power inductor [17] as an example here ($I_{sat} = 3.12A$ for 10% drop
in L value, 12mm*12mm*7.8mm in volume). Based on power loss data from [18], inductor core loss is considered by adding \( r_{eq} = 0.9\Omega \cdot f_{sw}/100kHz \) to \( P_{\text{trip}} \). Fig. 10 shows the power dissipation versus \( f_{sw} \) trend for the same load condition as in Fig. 8 (I\(_{\text{out}}\) = 400mA, D = 0.5). Compared with Fig. 8, \( P_{\text{trip}} \) takes up a higher portion of the total loss. Even though total dissipation has practically doubled by including core loss, minimum dissipation is achieved at only a slightly higher \( f_{sw} \). Therefore it can be concluded that operation on the SSw boundary leads to dissipation very close to minimum. This is the basis of the proposed frequency regulation technique.

C. Switching Frequency Regulation

To achieve minimum dissipation the amplifier has to be kept at the soft switching boundary, but as explained in section II, this point depends heavily on circuit parameters and operating point. However, the \( V_{\text{pwm}} \) level at the rising edges of \( V_{\text{HS}}/V_{\text{LS}} \) can be used to indicate if the amplifier is soft switching. The working principle is shown in Fig. 11. Fig. 11(a) shows the SSw waveforms, with \( I_{\text{trip}} \) larger than necessary (excessive \( P_{\text{trip}} \)) for eliminating \( P_{\text{sw}}+P_{\text{cap}} \). Both \( V_{\text{pwm}} \) transitions finish within the dead time \( t_d \) and are already at the other supply rail when \( M_{\text{HS}}/M_{\text{LS}} \) turns on. This means \( I_{\text{trip}} \) (and consequently \( P_{\text{trip}} \)) could be smaller by increasing \( f_{sw} \). On the other hand, for the PSSw case shown in Fig. 11(b), \( I_L \) is too small to charge \( C_{\text{par}} \) during \( t_d \), and the remaining \( V_{\text{pwm}} \) rising transition is accomplished by \( M_{\text{HS}} \). \( V_{\text{pwm}} \) is not yet at \( V_{\text{DDP}} \) when \( M_{\text{HS}} \) turns on, indicating the existence of \( P_{\text{cap}} \) and \( f_{sw} \) should decrease.

Based on this analysis, the optimal-efficiency \( f_{sw} \) adaptation is as follows: 1) When during both transitions \( V_{\text{pwm}} \) reaches the supply rail before the corresponding \( V_{\text{HS}}/V_{\text{LS}} \) rising edge, \( f_{sw} \) should increase 2) When for either transition, \( V_{\text{HS}} \) or \( V_{\text{LS}} \) rises before \( V_{\text{pwm}} \) reaches the supply rail, \( f_{sw} \) should decrease. By adapting \( f_{sw} \) such that either one of the \( V_{\text{pwm}} \) switching is at the SSw boundary while the other is fully lossless,
minimization of both $P_{sw}+P_{cap}$ and $P_{trip}$ is achieved. By further setting a $f_{sw}$ lower limit, the system naturally shifts to hard switching at high power, with minimized $P_{sw}+P_{cap}$.

IV. CIRCUIT IMPLEMENTATION

A. Overall topology

The implementation of the amplifier is shown in Fig. 12. In this realization, the amplifier is based on a 1st-order hysteretic self-oscillating loop [20], [21]. Alternative implementations can also use carrier-based topologies [1], by changing $f_{sw}$ of the triangle carrier, either continuously or through a frequency plan to control the spectral content. $f_{sw}$ is controlled by the hysteretic window voltage $V_{tune}$. The power output stage works with 80V $V_{DDP}$, an on-chip regulated 3.3V driver supply and has a 2-step level shifter that can handle supply bounce higher than the internal supply [8].

B. Switching Frequency Regulation Loop

The implemented $f_{sw}$ regulation loop together with circuit design parameters are shown in Fig. 13. The combined one-shot pulse and charge pump/loop filter generates a constant-step $\Delta V_{tune}$ of 30mV for controlling $f_{sw}$, regardless of the timing difference $\Delta t_1$ and $\Delta t_2$ between $V_{pwm}$ and $V_{HS}/V_{LS}$. Subsequently, since $f_{sw}$ is inversely proportional to $V_{tune}$, the 30mV $\Delta V_{tune}$ controls a $\Delta f_{sw}=-f_{sw,0}*(30mV/ V_{tune,0})$. With the differential $V_{tune}$ range ($V_{tune-range}$) set between 1.08V and 2.7V in this design, $f_{sw}$ can change 1/36 to 1/90 from its previous value in each switching cycle. When the amplifier is far away from the soft-switching boundary, the loop will regulate the switching frequency in the direction of minimizing $\Delta t_1$ and $\Delta t_2$. When the regulation loop reaches steady state, the output stage operates at borderline SSw/PSSw and the loop will oscillate between SSw and PSSw on a cycle by cycle basis. Since $f_{sw}$
alternates only 1% - 3% when reaching steady state, it can easily be concluded from Fig. 7, Fig. 8 and Fig. 9 that the switching frequency remains very close to optimal.

When regulating toward steady state, the $f_{sw}$ regulation loop is conceptually similar to a sigma-delta loop where the $V_{pwm}$ level detector can be regarded as the quantizer and the CP/LF as a first-order loop filter. Circuit simulations with large output current steps have been performed to verify that the $f_{sw}$ regulation loop step response is indeed stable.

Regarding the tracking speed of the $f_{sw}$ regulation loop, maximum $\frac{dV_{tune}}{dt} = f_{sw}^* \Delta V_{tune}$. For a sinusoidal $V_{tune}$ with amplitude $\frac{1}{2}V_{tune-range}$ this means that $f_{v_{tune,max}} = f_{sw}^* \Delta V_{tune} / (\pi V_{tune-range})$. For a sinusoidal input signal with $f_{sig}$, two regulating cycles are required, as shown in Fig. 14, resulting in $f_{sig,max} = f_{sw}^* \Delta V_{tune} / (2\pi V_{tune-range})$. With the chosen circuit design parameters the maximum $f_{sig}$ tracking ability is set at around 600Hz, but can be changed to facilitate other tracking speeds.

C. Circuits

Fig. 15 shows the $V_{pwm}$ level detection circuit. At the beginning of a transition, when $V_{pwm}$ is far (up to 80V) from the supply rail, $M_{LSC}/M_{HSC}$ shield the clamps $M_{LSD}/M_{HSD}$ from $V_{pwm}$. When $V_{pwm}$ is close to the supply rail, $M_{LSC}/M_{HSC}$ are in the linear region, such that $M_{1}/M_{4}$ can detect if $V_{pwm}$ is close (less than a $V_{TH}$) to the supply rail. Control signals $V_{LS\_detect}/V_{HS\_detect}$ are generated in the output stage with their rising edges time shifted compared to $V_{LS}/V_{HS}$ such that they only activate $M_{LSC}/M_{HSC}$ for half the switching cycle to prevent cross current flow from the supply. For proper control of $M_{LSC}$ and $M_{HSC}$, $V_{LS\_detect}/V_{HS\_detect}$ are referred to PGND and $V_{pwm}$ respectively with additional level shifter circuits. $M_{4}$ level shifts to logic levels referred to $V_{SSD}$. $M_{1}-M_{3}$ level shift in 2 steps to deal with the large (> 3.3V) on-chip PGND bounce.
Fig. 16 shows the UP/DN decision logic. The $V_{\text{pwm}}$ status is sampled at the rising edge of $V_{\text{HS}}/V_{\text{LS}}$ for switching noise immunity. The 1 shot for an $f_{\text{sw}}$ increase is activated if both $V_{\text{pwm}}$ transitions are finished in time while the 1 shot for an $f_{\text{sw}}$ decrease is activated if either transition is not.

Fig. 17 shows the charge pump/loop filter for $V_{\text{tune}}$ generation. Since $V_{\text{tune}}$ is at 2× the signal frequency $f_{\text{sig}}$ (when $I_{\text{out}}$ increases in either direction), $V_{\text{tune}}$ generation is fully differential for minimal 2nd-order distortion. For a wide $f_{\text{sw}}$ tuning range, $V_{\text{tune}}$ must be able to operate near the supply rails. To facilitate this, complementary buffers (M1 and M2) are used to measure the common-mode voltage of $V_{\text{tune},p}$ and $V_{\text{tune},n}$. Corresponding replica buffers (M3 and M4) are applied to the common-mode reference voltage $V_{\text{CM}}$.

V. MEASUREMENT RESULTS

The amplifier is implemented in a 0.14µm SOI-based BCD process. The chip photograph is shown in Fig. 18, with the die measuring 3.4mm×2.5mm. In the layout, the power stage and the control blocks are separated to avoid the high switching noise associated with the power stage [8] to interfere with the signal path. For chip packaging, the same design considerations apply, with the noisy power stage pins ($V_{\text{DDP}}$, $PGND$, $V_{\text{pwm}}$, gate driver $V_{\text{DD}}$) placed at one side of the packaged chip and the pins for the control blocks at the other side. For the PCB, current switching loops [1] are separated from the signal path, to minimize noise coupling to the signal.

For power efficiency measurements, a series-connected 23µF + 1.6Ω is used to model the piezo-actuator [7]. Because this load is mostly capacitive at $f_{\text{sig}}$, most of the power processed by the amplifier i.e. $V_{\text{out,rms}}*I_{\text{out,rms}}$ (VA), will not be delivered to the load. Therefore we observe the dissipation $P_d$ for showing the effectiveness of the $f_{\text{sw}}$ regulation. The dissipation $P_d$ gives insight into how good the power amplifier is in
handling the output current/voltage without dissipating too much itself. $P_d$ includes all
dissipation: power stage, inductor and control circuits. Fig. 19 shows the measured
dissipation of the amplifier for a 500Hz sine wave for three fixed $V_{\text{tune}}$ settings and one
with $f_{\text{sw}}$-regulation enabled at 80V $V_{\text{DDP}}$. The inductor is a Murata 1410478C 100$\mu$H
inductor with 7.8A saturation current. The control blocks use an external 12V $V_{\text{DD}}$ and
the power stage uses an external 80V $V_{\text{DDP}}$. Current drawn from both $V_{\text{DD}}$ and $V_{\text{DDP}}$
supplies are included in $P_d$. Fig. 19 clearly shows that the amplifier can adjust its $f_{\text{sw}}$
for lowest dissipation across the whole output power range. Idle power consumption
is 360mW while for the two lower $f_{\text{sw}}$ cases it is 440mW and 690mW, achieving a
reduction of 18% and 48%. At the highest output power, the amplifier dissipates
3.66W with adaptive $f_{\text{sw}}$ enabled, while for the two higher $f_{\text{sw}}$ cases it dissipates 4.5W
and 5.33W, equivalent to a dissipation reduction of 19% and 31% respectively.

THD+N at 80V $V_{\text{DDP}}$ with the 23$\mu$F + 1.6$\Omega$ load is displayed in Fig. 20, which is
below 1.3% for up to 45VA output power. In addition, THD+N is also shown in Fig. 21
with 60V $V_{\text{DDP}}$ where the trend is much clearer.

The trend for the THD+N performance can be explained as follows: 1) At low
output power, i.e. modulation depth $M < 0.05$, THD+N is inversely proportional to $f_{\text{sw}}$
(see Appendix A). When adaptive $f_{\text{sw}}$ is enabled, $f_{\text{sw}}$ is regulated to the highest
possible value, thus resulting in the largest THD+N. 2) When output power is
increased, the ripple will constitute a smaller part of the load current. And since the
output node is charged by $I_{\text{out}}-I_{\text{rip}}$ and discharged by $I_{\text{out}}+I_{\text{rip}}$, the switching waveform
becomes increasingly asymmetric at higher output powers [22] until it enters hard
switching, where the full dead time shows up as distortion. For fixed low switching
frequencies the ripple is high, so the distortion increase happens at larger output
powers. For the $f_{\text{sw}}$ regulated case, the amplifier is kept borderline soft switching,
always producing higher distortion. 3) For high output power (M > 0.2), THD+N for the three fixed V_{tune} settings remain similar. The main reason is that the relative distortion introduced by the power switches’ turn-on delay for V_{pwm} HSw transitions [23] is proportional to f_{sw}, while the loop gain for suppressing this error is also proportional to f_{sw} [24]. It remains unclear why the f_{sw} regulated case has higher distortion than the fixed frequency cases. For applications that require lower distortion, a higher-order feedback loop can be used, either for hysteretic feedback [25] or fixed carrier [26], [27] topologies.

A comparison with other high-voltage, high-power class-D designs is shown in TABLE IV. For comparison, efficiency with a non-capacitive load (12Ω resistor) is measured. The usage of a 12Ω resistor, which has an impedance comparable to a 23µF capacitor at 500Hz signal frequency, is mainly due to the maximum output current capability of the amplifier. In addition, for the capacitive load case we list an “efficiency” defined as V_{out,ms}*I_{out,ms}/(P_{d}+V_{out,ms}*I_{out,ms}) to show how efficient the amplifier is when handling the reactive power. The f_{sw}-regulation technique enables this design to achieve best-in-class peak efficiency while significantly outperforming the other amplifiers at lower output powers.

VI. CONCLUSIONS

For high-voltage class-D amplifiers, different dominating power loss mechanisms exist with changing output power level. Simultaneous reduction of the inductor ripple current induced loss and the switching-induced loss across the full output power range can be achieved with an optimal-efficiency-tracking switching frequency regulation loop. This is realized by detecting the output switching node voltage level at the turn-on transition of the power switches. The designed amplifier offers the high
peak efficiency of existing class-D designs, keeping heat sinks small, while offering significant energy savings at lower, much more prevalent, output powers.

**APPENDIX A**

For low output powers where \( I_{\text{out}} \ll I_{\text{rip}} \) and the two \( V_{\text{pwm}} \) switching transitions are both SSw (Fig. 11(a)), the inductor current \( I_L \) at the moment of a \( V_{\text{pwm}} \) low-to-high transition is \( I_{\text{out}} - I_{\text{rip}} \) while at the moment of a \( V_{\text{pwm}} \) high-to-low transition it is \( I_{\text{out}} + I_{\text{rip}} \). Suppose the parasitic capacitance \( C_{\text{par}} \) at \( V_{\text{pwm}} \) is linear, then the \( V_{\text{pwm}} \) low-to-high transition time \( t_{LH} \) and the \( V_{\text{pwm}} \) high-to-low transition time \( t_{HL} \) can be expressed as,

\[
t_{LH} = C_{\text{par}} V_{DDP} / |I_{\text{out}} - I_{\text{rip}}| \tag{A1}
\]

\[
t_{HL} = C_{\text{par}} V_{DDP} / (I_{\text{out}} + I_{\text{rip}}) \tag{A2}
\]

Due to this unsymmetrical \( t_{LH} \) and \( t_{HL} \), the \( V_{\text{pwm}} \) output has an error voltage compared to the ideal case as shown in Fig. 22. Within one switching cycle \( T = 1/f_{\text{sw}} \), the error voltage caused by \( t_{LH} \) and \( t_{HL} \) can be expressed as,

\[
V_{e,LH} = -0.5 V_{DDP} f_{\text{sw}} t_{LH} \tag{A3}
\]

\[
V_{e,HL} = 0.5 V_{DDP} f_{\text{sw}} t_{HL} \tag{A4}
\]

Combining A1-A4 and assuming \( I_{\text{out}} \ll I_{\text{rip}} \), the final error voltage \( V_e \) then will be,

\[
V_e \approx -C_{\text{par}} V_{DDP}^2 f_{\text{sw}} I_{\text{out}} / l_{\text{rip}}^2 \tag{A5}
\]

By further inserting the \( I_{\text{rip}} \) expression from (1),

\[
V_e \approx -4 I_{\text{out}}^2 C_{\text{par}} l_{\text{out}}^2 / [D^2(1-D)^2] \tag{A6}
\]

As we can see from (A6), \( V_e \) is proportional to \( f_{\text{sw}}^3 \) for the open-loop power stage \( V_{\text{pwm}} \) output. Considering that an ideal 1st-order hysteretic-feedback based loop has a loop gain proportional to \( f_{\text{sw}}^2 \) [24], the final closed-loop output error will be proportional to \( f_{\text{sw}} \) for low output power.
REFERENCES


Figure Captions:

Fig. 1. Basic topology of a high-voltage class-D power stage.

Fig. 2. Illustration of a $V_{\text{pwm}}$ hard switching transition, where $M_{\text{HS}}$ has to perform the transition with V-I overlap. In this case switching-induced loss results in $M_{\text{HS}}$.

Fig. 3. Illustration of a $V_{\text{pwm}}$ lossless soft switching transition, where the inductor current can fully charge $V_{\text{pwm}}$ to $V_{DDP}$ without resorting to the active devices $M_{\text{HS}}/M_{\text{LS}}$.

Fig. 4. Illustration of a $V_{\text{pwm}}$ transition partially completed by $M_{\text{HS}}$, resulting in $P_{\text{cap}}$. In this case the inductor current amplitude is not large enough to fully charge $V_{\text{pwm}}$ to $V_{DDP}$ within the dead time.

Fig. 5. Depending on the relative amplitude of $I_{\text{rip}}$ and $I_{\text{out}}$, it can be that both $V_{\text{pwm}}$ switching transitions are soft switching or one of the transitions is hard switching. (a) Bidirectional inductor current result in $V_{\text{pwm}}$ low to high transition being soft switching. (b) Unidirectional inductor current flowing out of the power stage result in $V_{\text{pwm}}$ low to high transition being hard switching.

Fig. 6. Comparison between analytical model and transistor-level simulation for the dissipation of the output stage. (a) $I_{\text{out}}=300\text{mA}$. (b) $I_{\text{out}}=400\text{mA}$.

Fig. 7. Modeled contribution of each dissipation source with varying switching frequency at low output power. $P_{\text{rip}}$ is the dominating dissipation source at low switching frequency. Its contribution can be minimized by moving to higher $f_{\text{sw}}$ where $P_{\text{g}}$ and $P_{\text{sw}}+P_{\text{cap}}$ are not yet significant ($I_{\text{out}}=100\text{mA}$, $D=0.5$).

Fig. 8. Modeled contribution of each dissipation source with varying switching frequency at medium output power ($I_{\text{out}}=400\text{mA}$, $D=0.5$).

Fig. 9. Modeled contribution of each dissipation source with varying switching frequency at high output power ($I_{\text{out}}=800\text{mA}$, $D=0.5$).
Fig. 10. Modeled total power dissipation with varying $f_{sw}$ when output power inductor loss is included ($I_{out}=400\text{mA}$, $D=0.5$).

Fig. 11. Using $V_{pwm}$ level information at the rising edge of $V_{HS}/V_{LS}$ to indicate whether the switching frequency is at the point for reaching minimum dissipation (a) Excessive $P_{trip}$, $f_{sw}$ should be increased (b) $P_{cap}$ exists, $f_{sw}$ should be decreased.

Fig. 12. Topology overview of the class-D amplifier with $f_{sw}$ regulation.

Fig. 13. Illustration of the implemented switching frequency regulation loop.

Fig. 14. Illustration of $f_{sig}$ limits with respect to $V_{tune}$ tracking speed.

Fig. 15. $V_{pwm}$ level detection circuit.

Fig. 16. UP/DN decision logic.

Fig. 17. Charge pump/loop filter circuit used for the $V_{tune}$ generation.

Fig. 18. Chip photograph of the class-D amplifier, the die measures 3.4mm×2.5mm.

Fig. 19. Dissipation measurements with 80V $V_{DDP}$, for $f_{sw}$ regulation enabled as well as for fixed $V_{tune}$ settings. For the fixed $V_{tune}$ cases, $f_{sw}$ is measured in idle.

Fig. 20. THD+N measurement results with the series-connected 23µF + 1.6Ω load, $f_{sig}$ = 500Hz , $V_{DDP}$ = 80V, for $f_{sw}$ regulation enabled as well as for fixed $V_{tune}$ settings. For the fixed $V_{tune}$ cases, $f_{sw}$ is measured in idle.

Fig. 21. THD+N measurement results with the series-connected 23µF + 1.6Ω load, $f_{sig}$ = 500Hz , $V_{DDP}$ = 60V, for $f_{sw}$ regulation enabled as well as for fixed $V_{tune}$ settings. For the fixed $V_{tune}$ cases, $f_{sw}$ is measured in idle.

Fig. 22. Illustration of open-loop output stage $V_{pwm}$ error when both $V_{pwm}$ transitions are SSw.

**Table Captions:**
TABLE I List of main dissipation sources in a class-D power stage.

TABLE II Summary of the parameters used in simulation.

TABLE III Parameters associated with the power DMOSFETs for dissipation calculation.

TABLE IV Performance summary and comparison with other high-voltage, high-power class-D amplifiers.
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Fig. 5, Fig. 6.
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Fig. 21. THD+N measurement results with the series-connected 23\mu F + 1.6\Omega load, \( f_{\text{sig}} = 500\text{Hz} \), \( V_{\text{DDP}} = 60\text{V} \), for \( f_{\text{sw}} \) regulation enabled as well as for fixed \( V_{\text{tune}} \) settings. For the fixed \( V_{\text{tune}} \) cases, \( f_{\text{sw}} \) is measured in idle.

Fig. 22. Illustration of open-loop output stage \( V_{\text{pwm}} \) error when both \( V_{\text{pwm}} \) transitions are SSw.

### TABLE I. LIST OF MAIN DISSIPATION SOURCES IN A CLASS-D POWER STAGE.

<table>
<thead>
<tr>
<th>Dissipation Type</th>
<th>Source</th>
<th>Analytical Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction loss</td>
<td>( P_{\text{con}} ) ( I_{\text{ouc}} ) conduction</td>
<td>(2)</td>
</tr>
<tr>
<td>Ripple loss</td>
<td>( P_{\text{rip}} ) ( I_{\text{rip}} ) conduction</td>
<td>(6)</td>
</tr>
<tr>
<td>Gate driver loss</td>
<td>( P_{\text{g}} ) ( \text{Charging/discharging the gate capacitance of } M_{\text{HS}}/M_{\text{LS}} )</td>
<td>(7)</td>
</tr>
<tr>
<td>Capacitive loss</td>
<td>( P_{\text{cap}} ) ( \text{Charging/discharging } C_{\text{par}} \text{ on } V_{\text{pwm}} ) by ( M_{\text{HS}}/M_{\text{LS}} )</td>
<td>(13)</td>
</tr>
<tr>
<td>Switching loss</td>
<td>( P_{\text{sw}} ) ( \text{During hard switching, } V-(I_L+I_r) ) overlap dissipated in the power switches</td>
<td>(13)</td>
</tr>
</tbody>
</table>
### TABLE II. SUMMARY OF THE PARAMETERS USED IN SIMULATION.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Stage Supply $V_{DDP}$</td>
<td>80V</td>
</tr>
<tr>
<td>Gate Driver Supply $V_{DD}$</td>
<td>3.3V</td>
</tr>
<tr>
<td>Output Inductance $L_{out}$</td>
<td>100µH</td>
</tr>
<tr>
<td>$V_{pwm}$ Duty Cycle</td>
<td>0.5</td>
</tr>
<tr>
<td>Dead Time $t_d$</td>
<td>100ns</td>
</tr>
<tr>
<td>DMOSFET’s size</td>
<td>56000µm/0.75µm</td>
</tr>
</tbody>
</table>

### TABLE III. PARAMETERS ASSOCIATED WITH THE POWER DMOSFETs FOR DISSIPATION CALCULATION.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>On resistance $r_{on}$ (DMOSFET W/L=56000µm/0.75µm)</td>
<td>560mΩ</td>
<td>On resistance of the DMOSFETs</td>
</tr>
<tr>
<td>Gate Charge $Q_g$</td>
<td>15nC</td>
<td>$2\int_{PGND}^{V_{DD}} C_g(V)dV$</td>
</tr>
<tr>
<td>$Q_o$</td>
<td>8.5nC</td>
<td>$\int_{PGND}^{V_{DD}} C_{par}(V)dV$ (Both $M_{HS}$ and $M_{LS}$ are off)</td>
</tr>
<tr>
<td>$Q_o$</td>
<td>28nC</td>
<td>$\int_{PGND}^{V_{DDP}} C_{par}(V)dV$ (M$_{HS}$ is on)</td>
</tr>
<tr>
<td>$Q_{rr}$</td>
<td>$[(I_{out}-I_{rip})/100mA] \cdot 1.5nC$</td>
<td>Reverse recovery charge ($I_{out}&gt;I_{rip}$)</td>
</tr>
</tbody>
</table>

### TABLE IV. PERFORMANCE SUMMARY AND COMPARISON WITH OTHER HIGH-VOLTAGE, HIGH-POWER CLASS-D AMPLIFIERS.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>This work</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[6]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Piezo Driver</td>
<td>Audio Amp.</td>
<td>Audio Amp.</td>
<td>Audio Amp.</td>
<td>Audio Amp.</td>
</tr>
<tr>
<td>$V_{DDP}$</td>
<td>80V</td>
<td>60V</td>
<td>20V</td>
<td>50V</td>
<td>18V</td>
</tr>
<tr>
<td>$P_{out,max}$/Channel (W)</td>
<td>45VA$^{(1)}$</td>
<td>45W$^{(2)}$</td>
<td>100W</td>
<td>20W</td>
<td>240W</td>
</tr>
<tr>
<td>Efficiency @ $P_{out,max}$</td>
<td>93%</td>
<td>91%</td>
<td>&gt;90%</td>
<td>89%</td>
<td>N/A</td>
</tr>
<tr>
<td>Efficiency @ 0.1* $P_{out,max}$</td>
<td>80%</td>
<td>84%</td>
<td>N/A</td>
<td>&lt;75%</td>
<td>N/A</td>
</tr>
<tr>
<td>Efficiency @ 0.01* $P_{out,max}$</td>
<td>49%</td>
<td>51%</td>
<td>N/A</td>
<td>&lt;30%</td>
<td>N/A</td>
</tr>
<tr>
<td>Idle Loss/Channel (w. output filter)</td>
<td>0.36W</td>
<td>1.6W</td>
<td>0.5W</td>
<td>2.1W</td>
<td>N/A</td>
</tr>
<tr>
<td>THD+N</td>
<td>0.015% (@9VA, $f_{sig}=100Hz$)</td>
<td>0.017% (@1W, $f_{sig}=1kHz$)</td>
<td>0.01% (@10W, $f_{sig}=1kHz$)</td>
<td>&lt;0.1%</td>
<td>0.7% (@13W, $f_{sig}=1kHz$)</td>
</tr>
</tbody>
</table>

$^{(1)}$ Load = 23µF+1.6Ω in series, efficiency = $V_{out,ms}*I_{out,ms}/(P_d*V_{out,ms}*I_{out,ms})$

$^{(2)}$ Load = 12Ω
Haifeng Ma received the BSc degree in Physics from Nanjing University, Nanjing, China, in 2007, and the MSc degree (with Honor) in Microelectronics from Fudan University, Shanghai, China, in 2010. From 2010 to 2014, he did his PhD research in the IC Design group at the University of Twente, Enschede, The Netherlands. His PhD thesis is on the design and optimization of integrated high-voltage class-D power amplifiers.

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He served as the Editor-in-Chief (2007-2010) of the IEEE Journal of Solid-State Circuits (JSSC), and was the 2013 program chair of the International Solid State Circuits Conference (ISSCC). Also he served as Associate Editor of IEEE Transactions on Circuits and Systems II (1997-1999), and of JSSC (2001-2006). He was in the Technical Program Committee of the Symposium on VLSI circuits (2009-2013) and is in the steering committee and programme committee of the European Solid State Circuit Conference (ESSCIRC). Moreover he is member of the ISSCC Executive committee. He served as distinguished lecturer of the IEEE, is elected member of IEEE-SSCS AdCom and is IEEE fellow. He is co-recipient of the ISSCC 2002 and 2009 “Van Vessem Outstanding Paper Award” and in 2014 he received the ‘Simon Stevin Meester’ award (500.000€), the largest Dutch national prize for achievements in technical sciences. In the same year he has been appointed as distinguished professor at the University of Twente.