Title: MULTIPROCESSOR COMMUNICATION SYSTEM

Abstract: The invention relates to a multiprocessor communication system (20) including at least two processors (21, 22) which are in communication with each other, the processors have network interfaces (24, 25) provided which are connected by means of a network data connection (26), wherein the respective network interfaces (24, 25) comprise at least one FIFO buffer (31, 32, 33, 34) and at least one register (27, 28, 29, 30) which indicates the existing data or the free space available within the FIFO buffer.
Multiprocessor Communication system

FIELD OF THE INVENTION

The invention relates to a multiprocessor communication system including at least two processors which are in data communication with each other, the processors have network interfaces provided which are connected by means of a network data connection as claimed in claim 1.

BACKGROUND OF THE INVENTION

Usually electronic systems communicate internally or with other systems such that a first data producing processor of the system exchanges data with a second data consuming processor of the system or of another system. Such communication takes place via so called peer-2-peer streaming interfaces while the data producing processor and the data consuming processor exchange data via a so called FIFO buffer or first in - first out buffer. Since the data producing processor has to feed the FIFO buffer the data producing buffer is stalled in case the buffer has no memory space or capacity to take data from the data producing processor. On the other hand the data consuming processor is stalled in case there are no data available in the FIFO buffer. As described there are several possibilities which reduce performance of the system due to lack of communication between the processors and the buffer.

Therefore a communication protocol is used to control communication between processors. Nevertheless the currently used DTL streaming protocol does not create or does not use signals which indicate how many word space is available within the FIFO buffer. Furthermore there is no signal provided which signals the available amount of words data within the FIFO buffer. As consequence in several cases a deadlock situation may occur in which the communication is stopped due to the above mentioned mechanism. With regard to performance of the system such a deadlock situation may reduce performance dramatically and therefore increases costs to achieve a certain degree of performance.

Furthermore US 4272819 discloses an inter-subsystem communication system in which a direct memory access is provided and additionally queue elements are provided which contain memory access information.

WO 91/11768 discloses a message transfer system for transferring messages between a master processor to a slave processor wherein a FIFO interconnection is provided.
OBJECT AND SUMMARY OF THE INVENTION

It is an object of the invention to create a multiprocessor communication system which improves the performance of such communication or mitigates the above described problems.

The object of the invention will be solved by a multiprocessor communication system according to the features of claim 1. The inventive multiprocessor communication system includes at least two processors which are in communication with each other, the processors have network interfaces provided which are connected by means of a network data connection, while the respective network interfaces comprise at least one FIFO buffer and at least one register which indicates the existing data or the free space available within the FIFO buffer.

According to the invention it is of advantage that at least one network interface comprises more than one register and/or more than one FIFO buffer. Furthermore it is of advantage that at least one network interface comprises two or more registers and/or two or more FIFO buffers which have the same a unique address in the memory map respectively.

Additionally according to another aspect of the invention a register indicates the available free data space or the sum of the available free data space.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other features and advantages of the invention will be apparent from the following description of an exemplary embodiment of the invention with reference to the accompanying drawings, in which:

Fig. 1 shows a diagram which illustrates a communication between two processors via a FIFO buffer; and

Fig. 2 shows a diagram which explains an embodiment of the inventive solution.

DESCRIPTION OF EMBODIMENT

Figure 1 shows a diagram 1 which explains the communication between two processors 2, 3 by means of a buffer 4. The buffer 4 is a so called FIFO buffer or First In - First Out buffer. Such FIFO buffers are known and they control the output of data 7 depending from the input 8 of the data. The processor 3, Proc 2, is able to and wants to read data 7 from the buffer 4 and issues a load instruction, which results in the generation of a load request, req signal high, which is represented by arrow 5. The processor 3 is stalled in
case there are no data available within the buffer 4 from the processor 1 which has not finalized to send data, what is represented by signal buffer empty high, see arrow 6. After the processor 3 has issued a load signal it can not perform a switch to another task until the load has been completed and all the data have been arrived at the processor 3. Accordingly the processor 3 is blocked for all other tasks and the performance is strongly reduced due to a waiting of the finishing of the loading process.

Furthermore the processor 2 will stall in case the FIFO buffer is completely filled and processor 2 can not send new data to the buffer as indicated by arrow 9.

On the other hand the data producing processor 2 may have to wait for input data of one of these tasks from processor 3 before the respective process or task of processor 1 can produce the required data and finally both processors are blocked and a deadlock situation occurs.

An inventive system provides a check by the processor whether there is space or there are data in the FIFO buffer to complete the task or process before a load or store process will be started. One possibility is to issue a load signal which polls whether there is space e.g. for one word or there are data available within the FIFO buffer. Accordingly the signal should be polled word by word which is written or stored within the buffer or which is read from the buffer.

Another inventive solution is described by way of the embodiment shown in Fig. 2. Fig. 2 shows a diagram 20 which shows a communication system between two processors 21, 22 which accordingly reveals two processors 21, 22 which are in data communication with each other by way of a network communication link 23. The network communication link 23 comprises a first network interface 24 and a second network interface 25 and a network connection 26. The first network interface 24 is preferably integrated within the network interface of the first processor 21 or is the interface of the first processor 21, while the first processor 21 is the data producing processor. The second network interface 25 is preferably integrated within the network interface of the second processor 22 or is the interface of the second processor 22, while the second processor 22 is the data producing processor.

As can be seen from Fig. 2 the network interfaces 24, 25 both have registers 27, 28, 29, 30 and FIFO buffers 31, 32, 33, 34. Each buffer has a respective register such that register 27 (reg1) is the respective register of FIFO buffer 31(FIFO1), register 28 (reg2) is the respective register of FIFO buffer 32(FIFO2), register 29 (reg3) is the respective register of FIFO buffer 33(FIFO3) and register 30 (reg4) is the respective register of FIFO buffer 34(FIFO4). In this case the value e.g. stored within the register may indicate an amount of data or data space or memory space available within the buffer e.g. next to the processor.
According to another embodiment the value within the register may indicate a sum of amount of data or a sum of space available for data within the buffers of one network interface.

According to the invention the registers and FIFO buffers of one network interface are memory mapped such that they have a unique address in the memory map. The value of information within the register 27, 28, 29, 30 indicates how many words of data or word space is available in the respective FIFO buffer 31, 32, 33, 34 preferably next to the processor 21, 22. This is of advantage if it is the objective to determine the execution time of the tasks independent of the latency and throughput settings of the network. These mentioned execution times of the system are of importance because they are input data of the design-time throughput and latency analysis techniques and therefore they are used as input data for special analysis techniques.

Finally after it has been determined using a polling process that there are data within the FIFO buffer 31, 32, 33, 34 or there is a certain amount of word space within the FIFO buffer 31, 32, 33, 34 the respective processor 21, 22 is able and ready for the subsequent writing process into the FIFO buffer 31, 32, 33, 34 or for a subsequent data reading process for reading data from the FIFO buffer 31, 32, 33, 34.

It is according to the invention not necessary that the processor 21, 22 fills the data space of the FIFO buffer 31, 32, 33, 34 completely or consumes the data space completely from the FIFO buffer 31, 32, 33, 34. Therefore a task can be pre-empted after each load process or store process and it is known at design-time how long it will take at most to complete a load process or a store process. This knowledge allows to create a system in which one task does not affect the progress of another task.

Furthermore the at least one of the registers 27, 28, 29, 30 is able to indicate what data are available in the provided FIFO buffers 31, 32, 33, 34 if it is the objective to guarantee that an above mentioned deadlock will not occur. The respective register 27, 28, 29, 30 may accordingly indicate the available space or the sum of the available space and/or respective credits.

In order to create a so called deadlock freedom, i.e. no deadlocks will occur, e.g. for so called best-effort applications only, the network may affect the execution time eventually of other tasks in an unpredictable manner because the consumption speed of the network will determine the progress of the load process of the respective task. During each load from the FIFO buffer the processor is unable to perform a change of a task or a switching of a task. Furthermore the time during which the loading process takes place and the length of this time of the loading may depend upon the production speed of the network,
but which is not defined for a so called a best-effort network. Therefore that may affect the performance of the communication system and the progress of other tasks.
REFERENCES

1 diagram
2 processor
3 processor
4 FIFO buffer
5 arrow
6 arrow
7 output of data
8 input of data
9 arrow
20 diagram
21 processor
22 processor
23 network communication link
24 network interface
25 network interface
26 network connection
27 register
28 register
29 register
30 register
31 FIFO buffer
32 FIFO buffer
33 FIFO buffer
34 FIFO buffer
CLAIMS:

1. Multiprocessor communication system (20) including at least two processors (21, 22) which are in communication with each other, the processors have network interfaces (24, 25) provided which are connected by means of a network data connection (26), characterised in that the respective network interfaces (24, 25) comprise at least one FIFO buffer (31, 32, 33, 34) and at least one register (27, 28, 29, 30) which indicates the existing data or the free space available within the FIFO buffer.

2. Multiprocessor communication system according to claim 1 wherein at least one network interface comprises more than one register (27, 28, 29, 30) and/or more than one FIFO buffer (31, 32, 33, 34).

3. Multiprocessor communication system according to claim 1 or 2 wherein at least one network interface comprises two or more registers (27, 28, 29, 30) and/or two or more FIFO buffers (31, 32, 33, 34) which have the same a unique address in the memory map respectively.

4. Multiprocessor communication system according to at least one of the preceding claims wherein a register (27, 28, 29, 30) indicates the available free data space or the sum of the available free data space.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV: H04L112/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<tr>
<th>Category</th>
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<td>X</td>
<td>WO 2005/093591 A (KONINKL PHILIPS ELECTRONICS NV [NL]; RADULESCU ANDREI [NL]; GOOSSENS K) 6 October 2005 (2005-10-06) page 10, line 15 - line 16; figures 1,2</td>
<td>1-4</td>
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☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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<thead>
<tr>
<th>Patent document cited in search report</th>
<th>Publication date</th>
<th>Patent family member(s)</th>
<th>Publication date</th>
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</thead>
<tbody>
<tr>
<td>WO 2005093591 A</td>
<td>06-10-2005</td>
<td>CN 1938695 A</td>
<td>28-03-2007</td>
</tr>
<tr>
<td>JP 2007531101 T</td>
<td></td>
<td></td>
<td>01-11-2007</td>
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<tr>
<td>KR 20070010127 A</td>
<td></td>
<td></td>
<td>22-01-2007</td>
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<tr>
<td>US 2008244136 A1</td>
<td></td>
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<td>02-10-2008</td>
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