Title: POLYPHASE HARMONIC REJECTION MIXER

Abstract: A polyphase harmonic rejection mixer, comprising a plurality of stages following each other; wherein a first stage is arranged to perform at least frequency conversion; and a second stage is arranged to perform at least selective weighting and combining; wherein at least two of the plurality of stages are arranged to perform at least combining. In an embodiment, the first stage (28) comprises three single-ended gain blocks (10, 12, 14), arranged to perform selective weighting, frequency conversion and combining; and a second stage (30) following the first stage (28) and arranged to perform selective weighting and combining. The second stage (30) may reduce the number of phases output by the first stage (28) and may output (32) a complex differential down converted signal. The mixer may be directly interfaced to an antenna of an LNA-less receiver without weighting in the first stage. The mixer may be included in a software-defined radio.
— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

— as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

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DESCRIPTION

POLYPHASE HARMONIC REJECTION MIXER

The present invention relates to polyphase harmonic rejection mixers and their operation. The present invention is particularly suited to, but not limited to, polyphase harmonic rejection mixers for use in wideband radio transceivers such as software-defined radio.

Harmonic rejection (HR) mixers allow a saving on radio frequency (RF) band-filtering to be made, for example in software-defined radio (SDR). Common implementations of HR mixers use a weighted combination of hard-switching mixers that need careful alignment of phase and gain parameters.

Switching mixers with rejection properties on one or more odd higher harmonics, also known as harmonic rejection (HR) mixers, are increasingly being used, especially in so called software defined radio. Frequency up or down conversion with a HR mixer enables a saving on RF filtering. Usually a HR mixer uses a weighted combination of hard-switching sub-mixers. The sub-mixers can be of the active (e.g. Gilbert) type or of the passive switching type.

The weighted combining of hard-switching mixers effectively creates a sinusoid-like mixing waveform. Figure 1 gives a schematic example of a conventional HR mixer suppressing the 3rd and 5th harmonic and Figure 2 shows the associated mixing waveforms of such a conventional HR mixer created by a weighted addition of 3 hard-switching mixer outputs.

To achieve a high amount of harmonic rejection ratio (HRR) requires careful alignment of the phase and amplitude of the segment contributions, as illustrated schematically in Figure 1. Vice-versa this makes HR mixers susceptible to gain and phase mismatch. Phase and gain mismatch can be
caused by process, voltage, and temperature (PVT) variations. In practical implementations of HR mixers the achievable HRR is usually limited to 30 to 40 dBc. To guarantee HRR beyond this range often needs a calibration.

Harmonic rejection mixer operation can be understood from the frequency spectrum of the resulting mixing waveform. Three rectangular signals p2, p0 and p1 together make up the mixing waveform, and are each phase shifted 45° and have amplitudes 1, $\sqrt{2}$ and 1 respectively, as shown in Figure 2. The rectangular signals each comprise a fundamental tone plus a large number of odd higher harmonics as illustrated by Figure 3 showing a unity amplitude square wave (indicated by reference numeral 2) and its frequency content (indicated by reference numeral 4). The vector contributions of 1st, 3rd, 5th, and 7th harmonics (shown in Tables 1a and 1b below), show how the different segment responses at the 3rd and 5th harmonic will cancel each other. In the presence of phase or amplitude errors the cancellation will not be perfect, as shown in Figure 4, where Figure 4 shows third harmonic rejection as a function of gain and phase error applied to signal p0 in Figure 2.

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<td>1/7</td>
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Table 1a

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<td>45</td>
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Table 1b

The present inventors have realised that it would be desirable to reduce the susceptibility of the mixer to the gain mismatch.

In a first aspect, the present invention provides a polyphase harmonic rejection mixer, comprising: a plurality of stages following each other; wherein a first stage is arranged to perform at least frequency conversion; and a second stage is arranged to perform at least selective weighting and
combining; wherein at least two of the plurality of stages are arranged to perform at least combining.

The polyphase harmonic rejection mixer may comprise one or more further stages, each further stage being arranged to perform selective weighting and combining.

The first stage may be further arranged to perform combining in addition to frequency conversion.

The first stage may be further arranged to perform selective weighting in addition to frequency conversion and combining.

A following stage may be arranged to reduce the number of phases output by its preceding stage.

The final stage may be arranged to output a complex differential down converted signal.

The frequency conversion may be implemented by mixers or samplers.

The combining may be implemented by resistance or transimpedance or digital blocks.

The selective weighting in one or more of the stages may be implemented by resistance or transconductance or digital blocks.

The selective weighting in at least one stage may be implemented by plural gain blocks.

The gain blocks may be single-ended or differential.

Each gain block may drive a respective set of plural mixers or samplers.

In a further aspect, the present invention provides an LNA-less receiver comprising an antenna directly interfaced to a polyphase harmonic rejection mixer according to any of the above aspects.

In a further aspect, the present invention provides a software-defined radio comprising a polyphase harmonic rejection mixer according to any of the above aspects.

In a further aspect, the present invention provides a method of polyphase harmonic rejection mixing, the method comprising: a first stage performing at least frequency conversion; and a second stage performing at
least selective weighting and combining; wherein at least two stages perform at least combining.

The method may further comprise one or more further stages each performing selective weighting and combining.

A following stage may reduce the number of phases output by its preceding stage.

Embodiments of the present invention will now be described, by way of non-limiting example only, and with reference to the accompanying drawings, in which:

Figure 1 schematically illustrates a conventional HR mixer that requires three LO phases;

Figure 2 shows an effective mixing waveform of a conventional HR mixer (3rd and 5th) created by a weighted addition of 3 hard-switching mixer outputs;

Figure 3 shows a unity amplitude square wave and its frequency content;

Figure 4 shows third harmonic rejection as a function of gain and phase error applied to a signal p0;

Figure 5 shows a general block diagram of an HR mixer having multiple stages;

Figure 6 shows an example of two-stage polyphase HR mixer;

Figure 7 shows the weighting factors for the 8-phase outputs of the first-stage HR versus time (t) for one complete period of the LO (T);

Figure 8 is a schematic representation showing certain principles and outcomes of two-stage polyphase harmonic rejection;

Figure 9 is a schematic illustration of an embodiment of a complex multi-stage polyphase HR mixer;

Figure 10 schematically illustrates a complex implementation of a conventional HR mixer that requires four LO phases;

Figure 11 schematically shows the 8 phased LO waveforms with 12.5% duty cycle used by HR mixer circuits of Figure 9 and Figure 12;
Figure 12 is a schematic illustration of a further embodiment of a multi-stage polyphase HR mixer;

Figure 13 is a schematic illustration of a further embodiment of a multi-stage polyphase HR mixer.

Figure 14 schematically shows the 8 phased LO waveforms with 50% duty cycle used by HR mixer circuits of Figure 13 and Figure 15; and

Figure 15 a schematic illustration of a further embodiment of a multi-stage polyphase HR mixer.

The present invention provides a multi-stage polyphase harmonic rejection mixer that tends to reduce susceptibility to gain mismatch, for example as shown in Figure 5. Another example is a two-stage polyphase HR mixer, as shown in Figure 6. This mixer suppresses the 3rd and 5th harmonics.

To achieve high HRR requires the accurate implementation of the desired weighting ratios, in this case the irrational ratio $1: \sqrt{2}:1$. The weighting ratios need be sufficiently close to their nominal (average) value and the effect of component mismatch on the weighting ratio needs to be sufficiently small. Both aspects are addressed by a two-stage polyphase HR concept. By distributing weighting and combining over 2 stages, Figure 6, a much higher HRR can be achieved than with traditional HR mixers using only one stage.

Figure 6 shows the block diagram of the two-stage polyphase HR mixer driven from an 8-phase LO signal for frequency conversion. The irrational ratio $1: \sqrt{2}:1$ is realized in two steps with integer ratios: a first step with 2:3:2 and a second step with 5:7:5. The 8-phase down conversion of the input RF signal in the first stage produces 8 IF output signals having equidistant phases, i.e., 0° to 315° with 45° step. This enables an iterative HR by adding a second stage that does a weighted combining of the 8-phase IF signal to the conventional I and Q quadrature differential outputs. To illustrate the operation further, Figure 7 shows the weighting factor for the 8-phase outputs of the first-stage HR versus time (t) for one complete period of the LO signal (T). If each time three adjacent-phase outputs of the first-stage are weighted and combined by
second-stage weighting factors 5:7:5, as shown in Figure 8, we find overall weighting of 29:41:29.

Figure 8 is a schematic representation showing certain principles and outcomes of the two-stage polyphase harmonic rejection. \( \alpha \) and \( \beta \) are errors in \( \sqrt{2} \) of the first stage and the second stage respectively, however the principles also apply to errors in 1:1 mismatch. The top part of Figure 8 shows a calculation of how \( \sqrt{2} \) is approximated to within 0.03% as 41:29 by simple integer 2:3:2 and 5:7:5 ratios. This 41:29 ratio in the effective LO amplitude is constructed via three signal paths, each with a weighting factor of the first stage (time-dependent factor 0, 2 or 3 in the array) and the second stage (constant 5 or 7). The bottom part of Figure 8 shows how for the desired signal, polyphase contributions from three paths add up, while for the 3rd and 5th harmonics, they cancel nominally. As the two stages are cascaded, the product of the gains determines the result. This means that the total relative error \( (\alpha \beta/4) \) is the product of the relative errors (first stage: \( \alpha/2 \), second stage: \( \beta/2 \)). If the second stage has 1% error (\( \beta \)), this advantageously improves HR by \((\beta/2)^{-1}\), i.e. 46dB compared to conventional arrangements.

For example, in tests on the above described complex two-stage polyphase HR mixer according to Figure 6 implemented on a receiver test chip, the minimum 3rd HR ratio over 40 samples measured was 60dB and 5th HR ratio 64dB. All even-order HRR were found to be greater than 60dB. As observed from multiple chips, the improvement from the first stage to the second stage is in the range of 20dB to 40dB for both 3rd and 5th harmonics.

Figure 9 is a schematic illustration of an embodiment of a multi-stage polyphase HR mixer 6, more particularly a complex two-stage polyphase HR mixer 6. This embodiment tends to reduce susceptibility to gain mismatch. The two-stage polyphase HR mixer 6 tends to reduce the gain error (due to e.g. mismatch or parasitic effects) to a product of gain errors (e.g. two times 1% becomes 0.01%). Furthermore, a distribution of weighting over two stages is provided and this also allows use of simple integer ratios to accurately approximate irrational numbers.
To assist with understanding of this embodiment, let us first consider the following. Figures 1 and 10 schematically illustrate conventional HR mixers suppressing 3rd and 5th harmonics. The mixer shown in Figure 1 needs three LO phases. The mixer shown in Figure 10, which is a complex implementation, needs four LO phases (135 equals -45 inverted). If the mixer shown in Figure 10 is implemented with balanced signals the number of LO phases increases to eight, four of which are unique and the other four can be derived by inversion of the first four LO signals. Figure 9 shows an embodiment of a HR mixer according to the invention which achieves a corresponding functionality as the conventional HR mixer shown in Figure 10. The new complex mixer also uses 8 LO phases to suppress the 3rd and 5th harmonics.

In Figure 9, the complex two-stage polyphase HR mixer 6 comprises a first stage 28. A single-ended input RF signal 8 is input to the first stage 28. The first stage 28 is a selective weighting, frequency conversion and combining stage. The selective weighting 281 is implemented as three single-ended gain blocks 10, 12, 14. The frequency conversion 282 is implemented by mixers 101-108; 121-128; 141-148. Each single-ended gain block 10, 12, 14 drives a respective eight mixers 101-108; 121-128; 141-148, i.e. the first single-ended gain block 10 drives a first set of eight mixers 101-108, the second single-ended gain block 12 drives a second set of eight mixers 121-128, and the third single-ended gain block 14 drives a third set of eight mixers 141-148. Such a set of eight mixers can be driven from a single amplifier as the duty cycle of the LO signal is 1/8, as shown schematically in Figure 11, where Figure 11 schematically shows the LO waveforms for the eight phases. The combining 283 reduces the 24 phased mixer signals to 8 phased signals. The 3 x 8 single ended mixers share the same 8 LO signals so there are 24 output signals with 8 different phases.

The complex two-stage polyphase HR mixer 6 further comprises a second stage 30. The second stage 30 is a selective weighting and combining stage. The second stage 30 follows the first stage 28. The selective weighting 301 is implemented by resistors. The combining 302 reduces the signals from eight to four phases to output a complex differential down converted RF signal,
the output location being indicated in Figure 9 by reference numeral 32. The eight phases provided by the first stage 28 create the amount of phase signals needed for the signal recombination in the second stage 30 so as to achieve a second order gain mismatch reduction.

The first stage 28 uses a gain-ratio of 2:3:2. The second stage 30 uses a gain-ratio of 5:7:5 (via resistor ratios 7:5:7 of which one set of resistors of resistor value ratio 7:5:7 are indicated by way of example by reference numerals 34, 36, 38 in Figure 9). The 45° phase shift comes from the eight-phase first stage down converted signal. An advantage offered by this embodiment is that the integer weighting ratios are more easily realized on a chip than the irrational number √2 required by the conventional HR mixer.

In overview, in this embodiment the HR mixer generates N signals with 360/N phase difference due to the differences in LO-phase. These N signals are weighted and combined to obtain again N phases (with harmonic rejection). This is done in the combining part 283 of the first stage 28 (but could also be implemented differently if voltage mixers are used). The weighting 301 and the combining 302 of the second stage 30 (5:7:5 resistors and second amplifier stage) repeats this process. In general this stage again produces N signals with 360/N phase difference and the weighting and combining can be repeated.

In the above described embodiment, the complex two-stage polyphase HR mixer 6 uses an eight phase LO (suppressing the 3rd and 5th harmonics besides all even-order harmonics). However, this need not be the case, and in other embodiments the complex two-stage polyphase HR may be implemented for other number of phases, e.g. if another number of harmonics needs to be suppressed.

In the above described embodiment, the complex two-stage polyphase HR mixer 6 operates from a 1/8 duty cycle LO signal. However, this need not be the case, and in other embodiments other duty cycle values may be used.

In the above described embodiment, the input RF signal is a single-ended input RF signal 8. However, this need not be the case, and in other
embodiments the input RF signal may be fully differential instead of single-ended.

In the above described embodiment, mixers are used to implement the frequency conversion. However, this need not be the case, and in other embodiments frequency conversion may be implemented using techniques other than mixers, for example samplers.

In the above described embodiment, transimpedance type of elements is used to implement the combining. However, this need not be the case, and in other embodiments combining may be implemented using techniques other than transimpedance, for example resistance or digital blocks.

In the above described embodiment, transconductance and resistance type of elements are used to implement the weighting. However, this need not be the case, and in other embodiments weighting may be implemented using techniques other than resistance or transconductance, for example inductors, capacitors, switched capacitor elements, or digital blocks.

In the above described embodiment weighting ratios of 2:3:2 and 5:7:5 are used. However, this need not be the case, and in other embodiments other weighting ratios may be used, including equal weighting ratios, e.g. 1:1:1.

In the above described embodiment, the second stage reduces the signals from eight to four phases to output a complex differential down converted signal. However, this need not be the case, and in other embodiments the second stage output may keep the same number of phases as the first stage output (e.g. for repeated weighted combining).

In the above described embodiment, two stages are provided in the polyphase HR such that two stages of polyphase signal selective weighting are combined. However, in other embodiments, yet more stages may be provided in the polyphase HR such that yet more stages of polyphase signal selective weighting are combined. For example, a polyphase HR with three stages may be provided. Thus, the various embodiments may generally be referred to as providing a multi-stage polyphase HR, i.e. not only two-stage ones.
In other embodiments numbers of phases other than 8 may be used, for example 16 phases.

The embodiments described use analog circuits to implement the selective combining of multi phased output signals. Instead, each of the mixer output signals may be applied to a respective Analog to Digital Converter and the further signal processing of selective weighting and combining implemented in the digital domain. An embodiment in which this is implemented is described later below with reference to Figure 15.

The above described embodiments of a complex polyphase HR mixer may be used in any mixer that uses or requires HR, i.e. any appropriate application, device or system. Examples include wide band broadcast receivers (TV), software defined radio, indeed any transceiver or other device requiring a harmonic rejection mixer. In particular, when used in a mixer that directly interfaces an antenna (e.g. a so-called LNA-less receiver), the two-stage (or other numbers of stages) approach offers benefit in that the influence of the varying antenna impedance on HR will tend to be strongly reduced.

Another advantage that tends to be provided, and mentioned in passing earlier above, is that the two-stage HR approach reduces the gain error (due to e.g. mismatch or parasitic effects) to a product of gain errors (e.g. 1% times 1% becomes 0.01%). The distribution of selective weighting over two stages also allows use of integer ratios to accurately approximate irrational numbers. These advantages also tend to apply to those embodiments with more than two stages.

Figure 12 is a schematic illustration of a further embodiment of a multi-stage polyphase HR mixer 42, more particularly a complex two-stage polyphase HR mixer 42. The HR mixer 42 is the same as the HR mixer 6 described above with reference to Figure 9, except that the selective weighting 281 of the first stage 28 is omitted (i.e. the three single-ended gain blocks 10, 12, 14 are omitted). The same reference numerals as used in Figure 9 are used again to indicate the same elements. Thus in this embodiment the first stage 28 is a frequency conversion and combining stage. This embodiment is particularly advantageous for LNA-less receivers.
Figure 13 is a schematic illustration of a further embodiment of a multi-stage polyphase HR mixer 44, more particularly a complex three-stage polyphase HR mixer 44. The HR mixer 44 has balanced signals and mixers operating from 50% duty cycle LO signals. Figure 14 schematically shows the LO waveforms for the eight phases. The first stage 46 is a frequency conversion stage, more particularly a multi-phase frequency conversion stage. The second stage 48 is a selective weighting and combining stage, and follows the first stage 46. The selective weighting 481 of the second stage 48 is implemented by resistors. The combining 482 of the second stage 48 reduces the phases from 24 to 8. The third stage 50 is a further selective weighting and combining stage, and follows the second stage 48. The selective weighting 501 of the third stage 50 is implemented by resistors. The combining 502 of the third stage 50 reduces the signals from eight to four phases to output a complex differential frequency converted signal, the output location being indicated in Figure 13 by reference numeral 52.

Compared to this HR mixer 44 described with reference to Figure 13, the HR mixer 6 described earlier above with reference to Figure 9 may be considered as an embodiment which saves components over the HR mixer 44, by introducing single ended mixers (driven with non-overlapping 12.5% duty cycle LO signals), moving the first stage weighting to the RF domain and, as a result, featuring a simplified first stage combining of mixer output currents in a low input impedance amplifier.

Figure 15 is a schematic illustration of a further embodiment of a multi-stage polyphase HR mixer 244, more particularly a complex three-stage polyphase HR mixer 244. The HR mixer 244 is the same as the HR mixer 44 described above with reference to Figure 13, except that digital circuits are used to implement the selective combining of multi phased output signals in the second stage 48 and the third stage 50, i.e. the second stage 48 and the third stage 50 are implemented in the form of digital circuitry. Each of the mixer output signals of the first stage 46 are applied to a respective Analog to Digital Converter 261, 262, 263, 264. The same reference numerals as used in Figure 13 are used again to indicate the same elements.
In each of the above embodiments, more than two signals are weighted and combined.
CLAIMS:

1. A polyphase harmonic rejection mixer, comprising:
   - a plurality of stages following each other; wherein
   - a first stage is arranged to perform at least frequency conversion; and
   - a second stage is arranged to perform at least selective weighting and combining;
   wherein at least two of the plurality of stages are arranged to perform at least combining.

2. A polyphase harmonic rejection mixer according to claim 2, comprising one or more further stages, each further stage being arranged to perform selective weighting and combining.

3. A polyphase harmonic rejection mixer according to claim 1 or 2, wherein the first stage is further arranged to perform combining in addition to frequency conversion.

4. A polyphase harmonic rejection mixer according to claim 3, wherein the first stage is further arranged to perform selective weighting in addition to frequency conversion and combining.

5. A polyphase harmonic rejection mixer according to any of claims 1 to 4, wherein a following stage is arranged to reduce the number of phases output by its preceding stage.

6. A polyphase harmonic rejection mixer according to any of claims 1 to 5, wherein the final stage is arranged to output a complex differential down converted signal.
7. A polyphase harmonic rejection mixer according to any of claims 1 to 6, wherein the selective weighting in one or more of the stages is implemented by resistance or transconductance or digital blocks.

8. A polyphase harmonic rejection mixer according to any of claims 1 to 7, wherein the selective weighting in at least one stage is implemented by plural gain blocks.

9. A polyphase harmonic rejection mixer according to claim 8, wherein the gain blocks are single-ended.

10. A polyphase harmonic rejection mixer according to claim 8 or 9, wherein each gain block drives a respective set of plural mixers or samplers.

11. An LNA-less receiver comprising an antenna directly interfaced to a polyphase harmonic rejection mixer according to any of claims 1 to 10.

12. A software-defined radio comprising a polyphase harmonic rejection mixer according to any of claims 1 to 10.

13. A method of polyphase harmonic rejection mixing, the method comprising:
   - a first stage performing at least frequency conversion; and
   - a second stage performing at least selective weighting and combining;
   wherein at least two stages perform at least combining.

14. A method of polyphase harmonic rejection mixing according to claim 13, further comprising one or more further stages each performing selective weighting and combining.
15. A method of polyphase harmonic rejection mixing according to claim 13 or claim 14, wherein a following stage reduces the number of phases output by its preceding stage.
Fig. 1 (PRIOR ART)

Fig. 2 (PRIOR ART)
Fig. 3 (PRIOR ART)

\[ s(t) = \frac{4}{\pi} \left( \cos \omega t - \frac{1}{3} \cos 3\omega t + \frac{1}{5} \cos 5\omega t - \cdots \right) \]
Fig. 15
**A. CLASSIFICATION OF SUBJECT MATTER**

**INV.** H03D7/16  H03D7/14

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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<td>WO 2009/006189 A2 (SILICON LAB INC [US]; RAFI ASLAMALI A [US]; PIOVACCARI ALESSANDRO [US]) 8 January 2009 (2009-01-08) figure 7</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

- **A** document defining the general state of the art which is not considered to be of particular relevance
- **E** earlier document but published on or after the international filing date
- **I** document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- **O** document referring to an oral disclosure, use, exhibition or other means
- **P** document published prior to the international filing date but later than the priority date claimed

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Name and mailing address of the ISA:
European Patent Office, P.B. 5818 Patentlaan 2
NL – 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer:
Agerbaek, Thomas
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