A clock with low phase-noise/jitter is a prerequisite for high-performance ADCs, wireless and optical data links and radio transceivers. This paper presents a 2.2GHz clock-generation PLL. It uses a phase-detector/charge-pump (PD/CP) that sub-samples the VCO output with the reference clock. The PLL does not need frequency divider in locked state and achieves a low in-band phase noise values at low power.

In a classical PLL, a VCO is locked to a reference clock Ref by a feedback loop with a divider, PD/CP, and loop filter. Both the VCO and the loop components contribute to PLL phase noise, the VCO noise dominating out-of-band and the loop noise in-band. In an optimized PLL, the two types of noise contribute equally to the output jitter [1, 2] and thus, are equally important. This work focuses on the loop noise and presents a technique to reduce it significantly. In most PLLs, the CP and the divider are the main sources of loop noise. The in-band CP noise, when transferred to the PLL output, is suppressed by the feedback gain from the PLL output to the CP output [1,2], denoted as $\beta_{\text{CP}}$. A larger $\beta_{\text{CP}}$ is preferred as it suppresses more CP noise. In a PLL using a conventional 3-state PFD/CP, the CP feedback gain is: $\beta_{\text{CP},3\text{state}}=I_{\text{CP}}/(2\pi N)$, with $I_{\text{CP}}$ the CP current and $N=f_{\text{VCO}}/f_{\text{Ref}}$.

The sampling-based PD was known for its high detection gain [3]. However, drawbacks like difficulty of integration (big filter capacitor) and limited pull-in range have prevented it from being widely used in PLLs [3]. Figure 23.2.1 shows the concept of the sub-sampling PD (SSPD) with a CP added. The key idea is to exploit the high dV/dt of the high-frequency VCO. The sine-wave VCO with amplitude $A_{\text{VCO}}$ and DC value $V_{\text{DC}}$ is directly sub-sampled by Ref, without using divider. The sampler output $V_{\text{samp}}$ controls a current $I_{\text{CP}}=g_{\text{m}}V_{\text{samp}}$, while a reference voltage $V_{\text{ref}}$ controls another current $I_{\text{CP}}=g_{\text{m}}V_{\text{DC}}$. If $N$ is an integer and the VCO and Ref are phase aligned, the sub-sampling renders $V_{\text{samp}}=V_{\text{DC}}$. The CP then outputs no current, and phase locking is achieved. If there are phase errors, they will be converted to voltage changes in $V_{\text{samp}}$ around $V_{\text{DC}}$, and then to current changes by the voltage-controlled CP. The ideal characteristic of the SSPD/CP has the same shape as the VCO output (see Fig. 23.2.1). In a PLL with this SSPD/CP, the CP feedback gain becomes $\beta_{\text{SSPD}}=A_{\text{VCO}}g_{\text{m}}$. Assuming, for simplicity, square-law MOS transistors equations can be used to calculate $g_{\text{m}}$ then: $\beta_{\text{SSPD}}=A_{\text{VCO}}(2L/V_{\text{gs,eff}})$, where $V_{\text{gs,eff}}$ is the effective gate-source voltage of the transistor. Comparing to $\beta_{\text{CP},3\text{state}}=I_{\text{CP}}/(2\pi N)$, $\beta_{\text{SSPD}}$ can easily be one order of magnitude larger as usually $N>>1$ and $A_{\text{VCO}}>V_{\text{gs,eff}}$. In other words, for the same $I_{\text{CP}}$, a PLL using a SSPD/CP has a much larger $\beta_{\text{CP}}$ than a PLL using a 3-state PFD/CP and thus suppresses CP noise more. Moreover, a PLL using a SSPD/CP does not need a divider in the locked state, which eliminates the noise and power contribution of the divider. As a result, the loop noise is greatly improved, which leads to a PLL design with low in-band phase noise at low power.

In a PLL, the optimal bandwidth for minimum jitter $f_{\text{opt}}$ is where the spectrum of the VCO and the loop noise intersects [1,2]. For lower loop noise, $f_{\text{opt}}$ is higher, requiring smaller loop-filter capacitors. Therefore, a larger $\beta_{\text{CP}}$ could also reduce chip area if the CP dominates the loop noise. However, if other loop components start dominating or if $f_{\text{opt}}$ reaches $f_{\text{Ref}}/10$, increasing $\beta_{\text{CP}}$ further can not increase $f_{\text{opt}}$ but does require a larger filter capacitor to stabilize the PLL. Such “unnecessarily high” $\beta_{\text{CP}}$ will not improve the loop noise but will make full integration difficult. In a PLL using a SSPD/CP, $\beta_{\text{CP}}$ can easily be “unnecessarily high”. Therefore, some way of gain control is desired.

The PLL chip is fabricated in a standard 1.8V 0.18µm CMOS process and occupies an active area of 0.4×0.45mm² (see Fig. 23.2.7). The IC is tested in a 24-pin LLP package with a 1.8V, 55MHz sine-wave Ref from a crystal oscillator. Figure 23.2.5 shows the measured phase noise of the 2.2GHz output from an Agilent E5501B phase-noise-measurement setup. The in-band phase noise at 200kHz offset is –126dBc/Hz. The total phase noise integrated from 10kHz to 40MHz is –56.8 dBc, which translates to an rms jitter of 0.15ps at 2.2GHz. The ~46dBc reference spur at 55MHz is caused by insufficient isolation between the VCO and the sampler, and can be improved in a re-design. Excluding the 50Ω CML buffer for measurement and disabling the 0.8mA PLL, the PLL core draws 4.2mA, with 1mA in the VCO. Figure 23.2.6 summarizes the PLL performance. Compared with [4–6], this design achieves the lowest jitter while consuming several times less power as well as active area. To make a fair comparison between in-band phase noise $L_{\text{in-band}}$ in PLL designs, the dependency of $L_{\text{in-band}}$ on $f_{\text{Ref}}$ and $N$ should be normalized out [7]. The normalized $L_{\text{in-band}}$ of this design is >12dB lower than that of [4–6], at a low loop power.

References:


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**Figure 23.2.1:** Principle and characteristic of a sub-sampling-based voltage-controlled PD/CP.

**Figure 23.2.2:** Sub-sampling PD/CP with pulse-width control.

**Figure 23.2.3:** Block diagram of the sub-sampling PLL.

**Figure 23.2.4:** Schematic of the sub-sampling PD/CP.

**Figure 23.2.5:** Measured PLL output phase noise. Reference spur at 55MHz is −46dBc, measured from a spectrum analyzer.

**Figure 23.2.6:** PLL performance summary and comparison with low-jitter PLL designs.
Figure 23.2.7: Chip micrograph.