Offset Cancelling Circuit

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Abstract — A monolithic offset cancelling circuit to reduce the offset voltage at an integrated audio-amplifier output is described. This offset voltage is detected using a low-pass filter with a very low time constant for which only one small on-chip capacitor is needed. The circuit was realized with a bipolar cell-based semicustom array.

Measurements have shown that a $3$-dB bandwidth below $5$ Hz can be realized with a capacitor value of $50$ pF. The resulting offset voltage at the audio-amplifier output was $2.5$ mV. The offset cancelling circuit increases the wide-band noise voltage at the audio-amplifier output by $0.15$-mV rms over the frequency range of $10$ Hz to $30$ kHz.

The use of the offset cancelling circuit eliminates the need for a large external electrolytic capacitor. If an audio amplifier with a single supply voltage is used, a second electrolytic capacitor, needed to obtain a stable reference at half the supply voltage, can be eliminated.

I. INTRODUCTION

In MOST integrated audio amplifiers the closed-loop gain is defined by a resistor ratio in the feedback loop as shown by Fig. 1. A problem is that the gain for an unwanted dc offset voltage equals the ac gain. Usually a capacitor is used to eliminate the dc gain as shown. However, large capacitor values are needed which cannot be integrated. Therefore there is a need for a fully integrated circuit that is capable of reducing the dc voltage at the audio amplifier output without influencing the amplifier operation in the audio frequency range.

In this paper a low-pass filter is described with a very low cutoff frequency ($<5$ Hz). Such a filter can be used as an offset cancelling circuit, but of course there are many other applications where low-frequency control loops are needed.

Straightforward RC techniques are incompatible with monolithic integration. For example, using an integrable capacitor of $50$ pF, a cutoff frequency of $5$ Hz requires a resistor value of $660$ MΩ. Based on a sheet resistance of $200$ Ω/μm and a resistor width/spacing of $5$ μm, we would need a resistor $16$ m long, requiring $160$-mm² chip area.

Large on-chip time constants can be electronically synthesized; however, a common problem is the occurrence of large noise and offset voltages. Electronic enhancement of a time constant often means a multiplication of noise and offset by the same factor, thereby reducing the dynamic range of the filter [1]. The circuit approach described here does not suffer from noise and offset multiplication. Class AB operation is applied to avoid large noise and offset values caused by large quiescent currents. A low-pass filter has been realized with a $3$-dB frequency of approximately $3$ Hz and an offset voltage of $2.5$ mV using one on-chip capacitor of $50$ pF and a total resistance value of $200$ kΩ. The wide-band noise voltage at the output of the filter, which is the extra noise that appears at the output of an audio amplifier that is corrected by the circuit, amounted to $0.15$-mV rms over the frequency range of $10$ Hz to $30$ kHz.

The paper is organized as follows. Section II explains the principle of the circuit. In Section III, the major building block is described—a $V-I$ converter with a very large input voltage range and low offset and transconductance. Section IV deals with the required attenuation of current using special current mirrors. The complete circuit is described in Section V. Measurement results are presented in Section VI for the circuit used as a low-pass filter and connected to an audio amplifier as an offset cancelling circuit. It is shown here that two large external electrolytic capacitors can be eliminated through use of a single integrated time constant. Finally, some conclusions are presented in Section VII.

II. CIRCUIT PRINCIPLE

Fig. 2 shows the principle of an audio amplifier with an offset cancelling circuit. The closed-loop gain in the audio frequency range is determined by the resistors $R_1$ and $R_2$. The voltage at the output of the amplifier is converted to a small proportional current. This current is fed to a Miller integrator. The integrated current results in a voltage $u_{corr}$ which is used to correct the offset voltage of the amplifier by adjusting its dc bias. It is assumed that a change $\Delta u_{corr}$ in $u_{corr}$ causes a change $\alpha \Delta u_{corr}$ in $u_{out}$.

Fig. 1. Audio amplifier with gain defined by the resistor ratio of $R_1$ and $R_2$.
Fig. 2. Audio amplifier with an offset cancelling circuit.

Fig. 3. Closed-loop Bode plot of the audio amplifier with offset cancelling circuit.

Fig. 4. The influence of $\alpha$ on $f_{-3\,\text{dB}}$.  

The voltage gain of the circuit as a function of frequency is given by

$$f_{-3\,\text{dB}} = \frac{1 + \alpha \cdot h_{fe} R_p \cdot g}{2\pi h_{fe} R_p C} = \frac{\alpha \cdot g}{2\pi C}, \text{  \text{ } } (\alpha \cdot h_{fe} R_p \cdot g \gg 1).$$

The offset voltage at the output of the circuit is given by

$$u_{\text{out,offset}} = \frac{R_1 + R_2}{R_2 \cdot (1 + \alpha \cdot h_{fe} R_p \cdot g)} \cdot u_{\text{offset 1}} + u_{\text{offset 2}}.$$  

The offset cancelling circuit should not influence the amplifier behavior in the audio frequency range. Therefore $f_{-3\,\text{dB}}$ should be below 10 Hz. So, for an integrated capacitor $C$, the transconductance $g$ must be extremely small.

As mentioned before, electronic enhancement of a time constant often means a multiplication of noise and offset by the same factor. To avoid noise and offset multiplication, it is necessary that any signal attenuation is attended by a noise and offset attenuation by the same factor. So, a small transconductance $g$ cannot be realized by subtracting the output currents of two $V-I$ converters with slightly different transconductances $g_1$ and $g_2$. In that case, the resulting transconductance $g$ would be $g_1 - g_2$, but the noise and offset of the two $V-I$ converters will in general not compensate each other. For the same reason, it is impossible to use a resistive divider at the input of the $V-I$ converter to attenuate the input voltage. In that case, both the offset and noise of the converter increase relative to the signal by the same factor.

So, in order to minimize any offset multiplication, the input stage of the $V-I$ converter should be able to handle the input voltages, which are nearly as high as the supply voltage, directly. In that case it is necessary to use class (A)B operation. Otherwise, the offset will be very high. This can be seen as follows. Without class (A)B operation, the quiescent currents in the circuit have to be at least as large as the maximum possible signal currents. Therefore the quiescent currents in the output stage of the $V-I$ converter will be at least $g \cdot V_S / 2$ ($V_S$ = supply voltage). Each percent error in the value of the current as a result of device inequalities will cause an extra offset equal to

$$\Delta u_{\text{out,offset}} = \frac{0.01 \cdot g \cdot V_S}{2 \cdot g} = 0.01 \cdot V_S / 2.$$  

For a supply voltage of 10 V this is already 50 mV. If class (A)B operation is used, the quiescent currents can be considerably smaller. A relative error in these currents will therefore lead to a much smaller input offset voltage.

At first it seems from (1) that $f_{-3\,\text{dB}}$ can be decreased by choosing $\alpha$ very small. However, it is of no use to make $\alpha$ smaller than 1, since this introduces low-frequency distortion. This can be seen as follows. Fig. 4 shows the voltage gains $|u_{\text{corr}}/u_{\text{out}}|$ and $|u_{\text{out}}/u_{\text{in}}|$ for $\alpha = 1$ and $\alpha < 1$. For $\alpha = 1$, $f_{-3\,\text{dB}}$ is equal to $f_1$. If $\alpha < 1$, $f_{-3\,\text{dB}}$ will be smaller than $f_1$. However, in that case the transfer ratio $|u_{\text{corr}}/u_{\text{out}}|$ becomes greater than 1 for all frequencies below $f_1$. In practice, however, $u_{\text{corr}}$ and $u_{\text{out}}$ are both restricted by the supply voltage. Therefore, the $u_{\text{corr}}$ signal will be hard-limited for low frequencies and large amplitudes of $u_{\text{out}}$. As a result, $u_{\text{out}}$ gets distorted. It follows that the optimal value for $\alpha$ is 1.

Substituting the value of $\alpha = 1$ in (1) and assuming a capacitor value of 50 pF gives the following condition for the transconductance $g$ of the $V-I$ converter to yield $f_{-3\,\text{dB}} < 10$ Hz:

$$g < \frac{2\pi \cdot k \cdot C \cdot f_{-3\,\text{dB}}}{\alpha} = 3 \cdot 10^{-9} \text{ A/V}.$$
A. Circuit Description

In addition to a very small transconductance, the $V-I$ converter should have a small input offset voltage and a large input voltage range. Also, a reasonable linearity over the entire input voltage range and good behavior over the entire audio frequency range are desirable. Nonlinearity or slew-rate limiting can cause a dc component in the output current if asymmetric input signals are supplied. This can also be the case with symmetric signals if the $V-I$ converter has an asymmetric slew rate or if the nonlinearity differs for positive and negative signal values.

Fig. 5 shows the schematic of a suitable class AB input stage for the $V-I$ converter. The input offset voltage of the circuit is primarily caused by mismatches between the transistors $T_1$ and $T_3$ and the resistors $R_E$. The offset caused by a difference in $R_E$ is proportional to the quiescent currents $I_1$ and $I_3$, which should therefore be small.

$I_1$ and $I_3$ are very small, because most of the bias current $I_0$ flows through $T_2$ [2]. It can be shown that the following relation exists between $I_0$ and $I_1$ (or $I_3$) if the base current of $T_2$ is neglected:

$$I_0 = (2e^{-qE_1/kT} + 1) - 2I_1. \quad (5)$$

The p-n-p transistors $T_2$ and $T_3$ become active only for large input signals and supplement the bias current $I_0$. In addition, these transistors protect $T_1$ and $T_3$ against base-emitter breakdown. For large $u_{in}$, the current through $T_3$ or $T_1$ equals

$$I_{T_3/1} = \frac{u_{in}}{2R_E} - \frac{U_{BE,T_3} + U_{BE,T_2}}{R_E}. \quad (6)$$

For large input signals only one of the transistors $T_3$ and $T_1$ conducts. The transconductance of the circuit is defined by the resistors $R_E$:

$$I_{out1} - I_{out2} = \frac{u_{in}}{2R_E}. \quad (7)$$

The transistors should be larger than this for all values of $u_{in}$. Therefore $I_0$ should be chosen larger than a minimum value given by

$$I_{0, min} = \frac{U_{BE,T_1} + U_{BE,T_2}}{R_E}. \quad (8)$$

In that case the value of $I_0$ does not impose a limit on the input voltage range which is then only limited by the supply voltage. $I_0$ should not be chosen very much larger than $I_{0, min}$ because $I_1$ and $I_3$, and therefore the offset voltage, increase with $I_0$.

$T_0$, $T_7$, and $R_{IN}$ provide some linearity correction for small input signals. This can be seen as follows. For small input signals, both $T_1$ and $T_3$ conduct. The transconductance of the circuit is influenced by the transistor transconductances. If we assume that $g_{m,T_1} = g_{m,T_3} = g_{m,T_2} = g_{m,T_0} = g_{m}$, it can be shown that the small-signal transconductance of the circuit will be equal to that for large input signals (7) if the following condition for $R_{IN}$ is satisfied:

$$\frac{1}{2} = \frac{qI_1}{kT} - R_{E} \cdot \frac{1/2}{qI_1 + kT} \cdot R_{E}. \quad (9)$$

So $R_{IN}$ can only be chosen optimal over a large temperature range if $I_1$ and $I_3$ vary proportionally with the absolute temperature. According to (5) this is the case if $I_0$ varies proportionally with the absolute temperature.

In summary, the $V-I$ converter operates in class AB, combining a low offset voltage with a large signal-handling capability. Its transconductance is given by $g = 1/2R_E$ and will be approximately linear when (9) is satisfied.

B. Dimensioning the $V-I$ Converter

The transconductance $g$ of the $V-I$ converter is determined by the emitter resistors $R_E$ and should be less than $3 \times 10^{-5} \text{ A/V}$. However, the large resistors needed to obtain this value cannot be realized on chip (160 MΩ would be needed). Pinch resistors cannot be matched very well and should not be used because a mismatch directly leads to an increase in offset. In view of a reasonable chip area 50-kΩ base-diffused resistors could be employed. In that case, the transconductance becomes approximately $1 \times 10^{-5} \text{ A/V}$ and a further current attenuation is therefore needed.

The current source $I_0$ should be proportional to the absolute temperature $T$ and larger than the minimum value given by (8). For $R_E = 50$ kΩ an acceptable value for $I_0$ is 35 µA at $T = 300$ K. From (5) it follows that $I_1$ and $I_3$ will be approximately 1.7 µA. So, the input offset voltage contribution caused by a 1-percent mismatch be-
between the emitter resistors $R_E$ will be $0.01 \times 50 \times 10^{-3} \times 1.7 \times 10^{-3} = 0.85 \text{ mV}$, which is acceptable.

The value of the base resistors $R_B$ is not critical as long as the voltage drop across these resistors caused by the base current of $T_2$ is small. A mismatch in $R_B$ does not cause an offset, although it causes asymmetrical output currents if an input signal is applied. For all measurements discussed below, we used a value of $7 \text{ k}\Omega$.

Finally, the value of $R_{lin}$ follows from (9) as approximately $60 \text{ k}\Omega$.

C. Measurements

The $V-I$ converter has been realized with our analog cell-based array (ACBA) semicustom chip [3], [4]. The resistors $R_{lin}$ and $R_E$ were connected externally to allow experimenting with their values. The differential output current $I_{out} = I_{M2} - I_{M1}$ and the transconductance have been measured as a function of the differential input voltage. The value of $V_{\text{REF}}$ was chosen equal to $V_S$, which was $18 \text{ V}$ (the maximum voltage allowed by the process).

The maximum allowable input voltage approximately equals the supply voltage. If a symmetrical input voltage is applied, signal amplitudes up to $36 \text{ Vpp}$ are possible. The circuit is well suited to be connected to the output of an audio amplifier. The transfer is linear, except for around the origin. Fig. 6 shows a plot of the measured transconductance $g$ over the input voltage range $-2$ to $+2 \text{ V}$ for various values of $R_{lin}$. For $R_{lin} = 56 \text{ k}\Omega$, we see that the small-signal transconductance is approximately equal to the large-signal transconductance, as expected. However, $g$ still varies approximately 15 percent with minima at $|V_{M}| = 0.4 \text{ V}$.

The input offset voltage was measured for a small number of samples and amounted to approximately $0.5 \text{ mV}$.

IV. ATTENUATING CURRENT MIRRORS

As stated in Section II the transconductance of the $V-I$ converter should be less than $3 \times 10^{-9} \text{ A/V}$. The transconductance of the circuit described in the previous section is approximately equal to $1 \times 10^{-7} \text{ A/V}$, so a further current attenuation by at least a factor 3300 is needed. In this section a pair of attenuating current mirrors is described which can be used for this purpose.

Fig. 7 shows the schematic of the current mirrors and a control circuit. The current mirrors consist of n-p-n input transistors (T8, T9) and p-n-p output transistors (T20, T21). The control circuit behaves like a voltage source $U$ at the emitters of the output transistors. The use of p-n-p output transistors makes it possible to use a n-p-n current mirror following the circuit. The latter is important because the output currents of the circuit are very small and a p-n-p current mirror would perform much worse, particularly with respect to leakage currents.

P-n-p input transistors could not be used because their voltage-to-current relation is not truly exponential for currents larger than $10 \mu\text{A}$. This is illustrated by Fig. 8. The figure shows the measured current attenuation for a p-n-p and a combined n-p-n/p-n-p current mirror with a constant voltage source at the emitter of the output transistor. The p-n-p mirror is highly nonlinear because lateral p-n-p transistors behave as if resistors are placed in series with their emitters (high injection). This effect is negligible if the combined mirror is used.
The total current attenuation factor of the mirrors in Fig. 7 is given by

$$\frac{I_{\text{out}1}}{I_{\text{in}1}} = \frac{I_{\text{out}2}}{I_{\text{in}2}} = \frac{I_{s,\text{pp}}}{m \cdot I_{s,\text{npn}}} \cdot e^{-\frac{V}{kT}}. \tag{10}$$

The voltage $U$ is the voltage drop across $R_1$, which is determined by the currents $I_1$ and $I_2$ as follows:

$$\frac{I_1}{I_2} = \frac{p \cdot I_{s,\text{pp}}}{I_{s,\text{npn}}} \cdot e^{-\frac{V}{kT}}. \tag{11}$$

A second relation between $I_1$ and $I_2$ is defined by the current amplifier consisting of $T_{10}$ to $T_{15}$:

$$I_2 = (r \cdot (n+1) + n) \cdot I_1. \tag{12}$$

Combination of (10)–(12) gives

$$\frac{I_{\text{out}1}}{I_{\text{in}1}} = \frac{I_{\text{out}2}}{I_{\text{in}2}} = \frac{1}{m \cdot p \cdot (r \cdot (n+1) + n)}. \tag{13}$$

So the attenuation is completely defined by the emitter areas of $T_6$, $T_{18}$, $T_{19}$, $T_{12}$, and $T_{14}$ and is independent of temperature. It is interesting to note that it is not necessary for the current $I_1$ to be much larger than $I_{\text{out}1} + I_{\text{out}2}$. The circuit works as long as the voltage drop caused by the sum of the output currents is smaller than the voltage drop that is needed for the desired current attenuation, according to (11). Similarly, the circuit is not sensitive to the absolute value of $R_1$.

In our circuit we have $I_{\text{out}1} + I_{\text{out}2} \ll I_1$. Therefore $U$ is given by $I_1 R_1$. Combination of (11) and (12) then gives

$$I_1 = \frac{kT}{qR_1} \ln \left( r \cdot (n+1) + n \right) \cdot \frac{p \cdot I_{s,\text{pp}}}{I_{s,\text{npn}}} \cdot e^{-\frac{U}{kT}}. \tag{14}$$

Therefore $I_1$ and $I_2$ vary proportionally with the absolute temperature $T$ if the ratio $I_{s,\text{pp}}/I_{s,\text{npn}}$ is not too strongly temperature dependent. This can conveniently be used to realize the PTAT current source $I_1$ required in Fig. 5. A certain spread or temperature dependence of $I_{s,\text{pp}}/I_{s,\text{npn}}$ only weakly finds expression in the value of $I_1$ because of the logarithm.

The transistors $T_{16}$ and $T_{17}$ and resistor $R_3$ form a starting circuit to eliminate the possibility that $I_1 = I_2 = 0$.

V. COMPLETE CIRCUIT

Fig. 9 shows the schematic of the complete offset cancelling circuit. The previously described $V-I$ converter with attenuating current mirrors is used followed by an n-p-n current mirror ($T_{24}$ and $T_{25}$). The resulting difference current is fed to a Miller integrator consisting basically of a Darlington pair ($T_{36}$ and $T_{37}$) with a constant current source at its collector and a capacitance between base and collector. The value of the current source is chosen in order that the dc-bias current needed at the base of $T_{36}$ approximately equals the sum of the base currents of $T_{24}$ and $T_{25}$ to compensate the offset voltage caused by these base currents. Of course, this compensation is only optimal if no input signal is applied. The base currents of $T_{24}$ and $T_{25}$ vary with the input voltage and a signal-dependent offset will occur. The output voltage of the integrator is buffered by $T_{42}$ and $T_{43}$. $T_{26}$ and $T_{28}$ are added to minimize collector–base leakage currents of $T_{25}$ and $T_{36}$, respectively. The collector-to-substrate leakage currents in $T_{24}$ and $T_{25}$ are not compensated. They are approximately of equal value and the resulting offset will be small as long as the leakage currents are small with respect to the quiescent currents through the transistors.

The transistors $T_{22}$ and $T_{23}$ are added to prevent turn-off...
effects in the current mirror caused by class AB operation of the $V-I$ converter. This improves the circuit performance with respect to large-signal distortion.

The circuit was both breadboarded and integrated on our semicustom ACBA [3], [4]. An on-chip capacitor of 50 pF was used. The emitter resistors $R_{E1}$ and $R_{E2}$ and the linearizing resistor $R_{lin}$ were connected externally to allow experimenting with their values. The attenuating current mirrors were dimensioned to attenuate by a factor 6000 by choosing $m = 10$, $n = 10$, $r = 10$, and $p = 5$ (see (13)). Therefore the total transconductance $g$ of the $V-I$ converter is expected to be $1.7 \times 10^{-9}$ A/V. The quiescent values of the output currents of the attenuating current mirrors are very small ($\approx 0.3$ nA). These currents can be increased while maintaining the same $-3$-dB frequency and offset if a larger integrating capacitor is allowed.

VI. EXPERIMENTAL RESULTS

A. Low-Pass Filter Application

The circuit in Fig. 9 has been tested on its own by connecting the output $u_{corr}$ to the inverting input as shown in Fig. 10. In that case the circuit behaves like a first-order low-pass filter. The offset voltage and $-3$-dB frequency of this filter are equal to $u_{offset}$ and $f_{-3 \text{ dB}}$ in Section II of this paper. All measurements were carried out at a supply voltage of 18 V, which was the maximum allowable voltage for the process used.

The total current consumption of the circuit with no signal applied was approximately 1.1 mA, of which 1 mA was caused by the current source $I_1$ in the output buffer.

The value of $u_{offset}$ has been measured for different values of $u_{in}$ as the difference $u_{in} - u_{corr}$. The offset voltage was approximately 2.5 mV over the entire output range (approximately $-7$ to $+6$ V with respect to $V_C/2$; determined by the output stage).

The voltage gain of the circuit has been measured as a function of the frequency. This has been done for the filter in two ways: 1) with $u_{corr}$ connected directly to the inverting input, and 2) with a voltage buffer (LM310) connected in series with $u_{corr}$. The results are shown in Fig. 11. The measurements without the voltage buffer show that the output stage of the circuit is not well suited to drive the inputs directly since the input signal feeds through to the output via the base resistors $R_p$ (see Fig. 9). However, this is not very important in our case, because if the circuit is used as an offset cancelling circuit the inputs will be driven by the audio-amplifier output which has a very low output resistance. The $-3$-dB frequency was measured as 3 Hz. This is less than the value expected from (1).

Due to the current mirror $T_{24}/T_{25}$, the circuit is not fully symmetrical and a dc component occurs at the output if a signal is applied (signal-dependent offset). The gain of the current mirror is slightly less than unity because of the base currents so a positive offset $u_{in} - u_{out}$ can be expected, dependent on the amplitude of the input signal. This dc component has been measured as a function of the input signal amplitude and frequency. The results showed that for frequencies below 10 kHz the dc component increases approximately linearly (12 mV/V) with the input signal amplitude. For frequencies above 10 kHz the offset voltage increases more than linearly.

The dependence of $f_{-3 \text{ dB}}$ and $u_{offset}$ on temperature has also been measured. The results are shown in Fig. 12. The $-3$-dB frequency only decreases slightly over the temperature range from 20 to 120°C. $u_{offset}$ remains substantially constant up to 110°C and increases slightly up to a value of 4 mV at 120°C. For higher temperatures the leakage currents (especially the collector to substrate leakage currents in $T_{24}$ and $T_{25}$) increase to the same order of magnitude as the collector currents of $T_{20} - T_{23}$ ($\approx 0.3$ nA) and then the offset increases drastically.

Finally, the rms amplitude of the wide-band noise voltage and the noise spectrum at the output of the filter have been measured. The rms amplitude amounted to approximately 0.15 mV over the frequency range of 10 Hz to 30 kHz. The measured noise spectrum is shown by graph 1 in Fig. 13. It can be seen that the noise level increases...
significantly for frequencies below 10 kHz. It has been found that this is caused by the low current level in the Miller integrator. This current was increased by connecting an extra current source to the emitter of $T_{29}$. The rise in offset caused by this was then compensated by adding two current sources to the emitters of $T_{11}$ and $T_{19}$. Graphs 2 and 3 in Fig. 13 show the noise spectrum for current levels in the Miller integrator of two and four times the normal level, respectively. The low-frequency noise level decreases considerably. However, the rms amplitude of the wide-band noise voltage over the frequency range of 10 Hz to 30 kHz only decreases slightly because of the increase of higher frequency noise components. The noise at the output of the filter will appear at the output of an audio amplifier which is corrected by the offset cancelling circuit.

B. Offset Correction Application

The circuit has also been tested in combination with operational amplifiers. Fig. 14 shows how the circuit was connected to the amplifiers. A dual supply voltage was used. Measurements have been carried out with a 741 operational amplifier and a TDA1514 integrated high-quality audio amplifier [6] at a closed-loop gain of 100 and 32, respectively. In both cases the closed-loop gain was measured as a function of frequency. The results are shown in Fig. 15. The effect of the offset cancelling circuit is exactly as expected: the gain decreases for low frequencies. The $-3$-dB frequency has been measured as 3 Hz. This is the same as in the case that the circuit is connected as a low-pass filter.

The dc offset voltage became in both cases approximately 2.5 mV, as in the low-pass filter application. A dc voltage at the input of the amplifier hardly affected the offset voltage up to the value where $u_{corr}$ gets limited by the supply voltage. Without the offset cancelling circuit the 741 operational amplifier had an output offset voltage of 150 mV and the TDA1514 had an output offset of 80 mV. If a signal is present at the amplifier output a dc component occurs as could be expected from the measurements on the offset cancelling circuit connected as a low-pass filter. The rise in signal-dependent offset shown for frequencies above 10 kHz does not occur in the circuit with the 741 operational amplifier, because the gain for those frequencies is already very small. The effect did occur in the circuit with the TDA1514 amplifier. If high-frequency components are present in the audio signal, special measures should be taken to prevent those components from reaching the input of the offset cancelling circuit. A possible solution would be to place a 10-kHz low-pass filter in front of the circuit.

If the offset cancelling circuit is used as shown in Fig. 14 one electrolytic capacitor normally placed in series with $R_2$ is eliminated (see also Fig. 1). Fig. 16 shows that for amplifiers with a single supply voltage a second electrolytic capacitor normally connected between node $X$ and ground to obtain a stable $V_s/2$ voltage can also be eliminated. However, the audio-amplifier inputs should be able to handle signals near ground potential. The closed-loop gain of the audio amplifier is defined by the resistors $R_1$ and $R_2$, as in Fig. 14. The output voltage of the offset cancelling circuit is now connected to the noninverting input of the audio amplifier via a resistive divider ($R_3, R_4$). The ratio $R_3/R_4$ has to be equal to $R_1/R_2$ to realize a factor $\alpha$ (see Section II) equal to unity. The input signal is con-
nected to $R_4$ and is therefore slightly attenuated by the divider $R_5$, $R_6$. The offset cancelling circuit will keep the output of the audio amplifier at half the supply voltage, due to the divider $R_5/R_6$. Ripple on the supply voltage will be filtered, just as the output signal of the amplifier. The circuit was constructed with a CA3140 operational amplifier representing the audio amplifier and $R_1 = R_2 = 26 \, \text{k}\Omega$, $R_5 = R_4 = 820 \, \Omega$, and $R_3 = R_6 = 1 \, \text{k}\Omega$. A 100-Hz ripple on the supply voltage $V_S$ appeared at the output attenuated by 37 dB as could be expected from Fig. 11 if the factor 2 attenuation of the voltage divider $R_5/R_6$ is also taken into account.

VII. Conclusion

A monolithic offset cancelling circuit to reduce the offset voltage at an integrated audio-amplifier output has been described. It has been shown that a $-3$-dB frequency below 5 Hz can be achieved using only one small on-chip capacitor of 50 pF and a total resistance value of 200 kΩ. The resulting offset voltage at the audio-amplifier output was approximately 2.5 mV and remained small up to a temperature of 120°C. For higher temperatures the leakage currents increase to the same order of magnitude as some of the quiescent currents and the offset rises drastically. The rms amplitude of the extra noise caused by the circuit at the audio-amplifier output amounts to approximately 0.15 mV over the frequency range of 10 Hz to 30 kHz. The circuit approach described is capable of handling large input voltages, restricted only by the supply voltage.

If the circuit is used in combination with an audio amplifier the capacitor usually used in the feedback loop to eliminate dc gain will be eliminated. If the dc voltage at the output of the circuit preceding the audio amplifier is not too large, the input capacitor can also be omitted. In addition, for amplifiers with a single supply voltage, a second capacitor used to obtain a stable $V_S/2$ voltage can be eliminated.

The circuit has a disadvantage in the form of a signal-dependent offset. The sinusoidal signal applied to the input of the circuit gives rise to a dc component at the output equal to approximately 1.2 percent of the signal amplitude because the circuit is not fully symmetrical. For signal frequencies above about 10 kHz the signal-dependent offset rises significantly and if the circuit is to be used in high-quality equipment, measures should be taken to prevent high-frequency signals from reaching the circuit input. A possible solution would be to place a 10-kHz low-pass filter in front of the circuit.

It might very well be possible to improve the circuit. The major cause for the signal-dependent offset are the base currents in the current mirror $T_{34}/T_{35}$. An extra transistor could be used to decrease this effect. In that case it might also be advantageous to interchange the collectors and emitters of $T_{34}$ and $T_{35}$. This will eliminate the collector-to-substrate leakage and decrease the collector-to-base leakage currents. In addition, parasitic capacitances will become smaller which probably improves the circuit behavior above 10 kHz.

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References


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