A low power frequency synthesizer circuit for a radio transceiver, the synthesizer circuit comprising:

- a digital controlled oscillator configured to generate an output signal \( f_o \) having a frequency controlled by an input digital control word (DCW);
- a feedback loop configured to provide the digital control word to the input of the digital controlled oscillator from an error derived from an input frequency control word (FCW) and the output signal; and
- a duty cycle module connected to the digital controlled oscillator and the feedback loop, the duty cycle module configured to generate a plurality of control signals to periodically enable and disable the digital controlled oscillator for a set fraction of clock cycles of an input reference clock signal (RefClock).

17 Claims, 8 Drawing Sheets